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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

OXFORD 2 14"
(BSW) 8PCS
WS BUILD

2016.08.24

21-OCT-2002		
DATE	CHANGE NO.	REV

DESIGN/DRAWER		XXX		DATE		21-OCT-2002		INVENTEC			
CHECK								TITLE MODEL PROJECT FUNCTION			
APPROVAL											
FILE NAME		CALTECH OXFORD						SIZE	CODE	DOC NUMBER	REV
PCB PIN		XXXXXXXX		PCB VER		AXI		SHEET	of	1	4B

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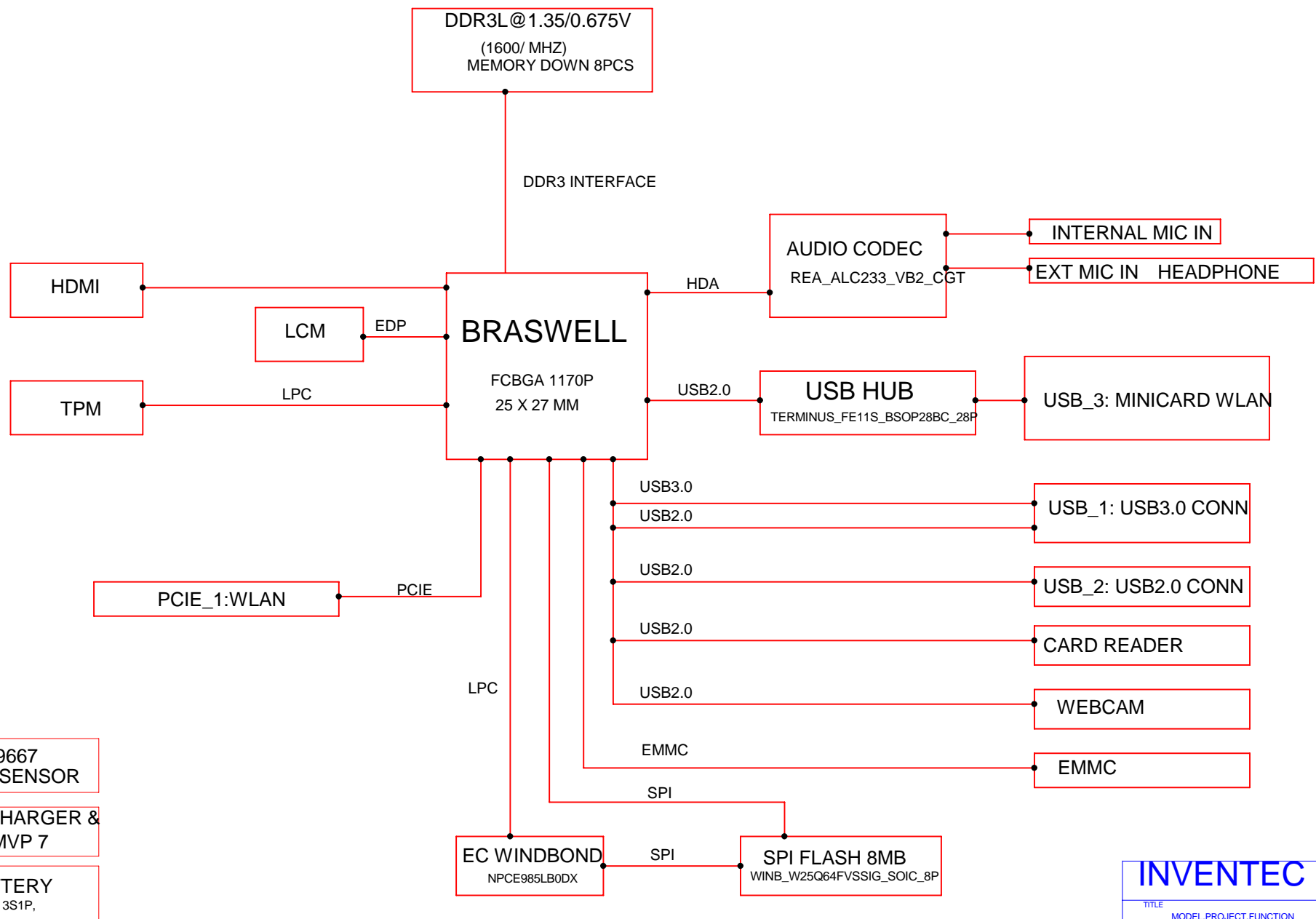
PAGE	PAGE
1. COVER PAGE	27. HDMI
2. INDEX	28~29.DDR3L
3. BLOCK DIAGRAM	30. THERMAL&DDR RESISTER
4. POWER MAP	31~32.DDR3L
5. POWER CHARGER	33. DDR RESISTER
6. POWER +V3.3A/+5A	34~43. CHIPSET
7. POWER +V1.35S	44. SVID
8. POWER VCORE	45. LEVEL SHIFT
9. POWER VCORE/MOS	46. EMI
10. POWER PVGG	47. USB2.0 DB
11. POWER PVGG/MOS	48. PWRBUTTON DB
12. MOIC(1V8.1V05.1V5.1V24.1V15)	
13. ENABLE PIN	
14. LOAD SWITCH	
15. PCB SCREW	
16. KB&TOUCH PAD&POWER DB CONN	
17. EC	
18. AUDIO CODEC	
19. SPEAKER/HP JACK/MIC JACK	
20. CARDREADER	
21. NGFF WLAN/DEBUG CARD	
22. USB2.0 DB CONNECTOR	
23. USB3.0	
24. EMMC	
25. TPM	
26. EDP	

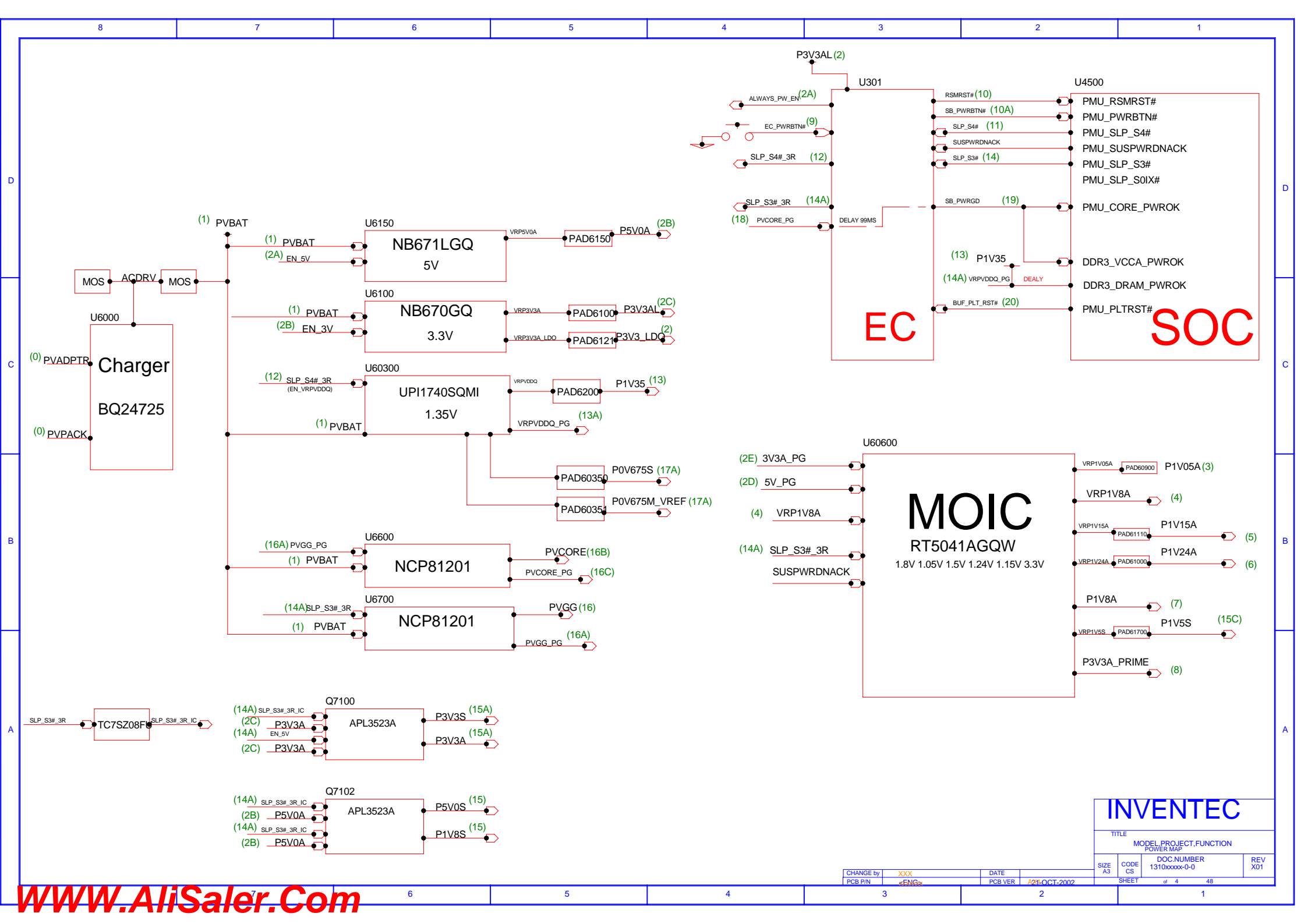
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TITLE
MODEL,PROJECT,FUNCTION
CATELOG

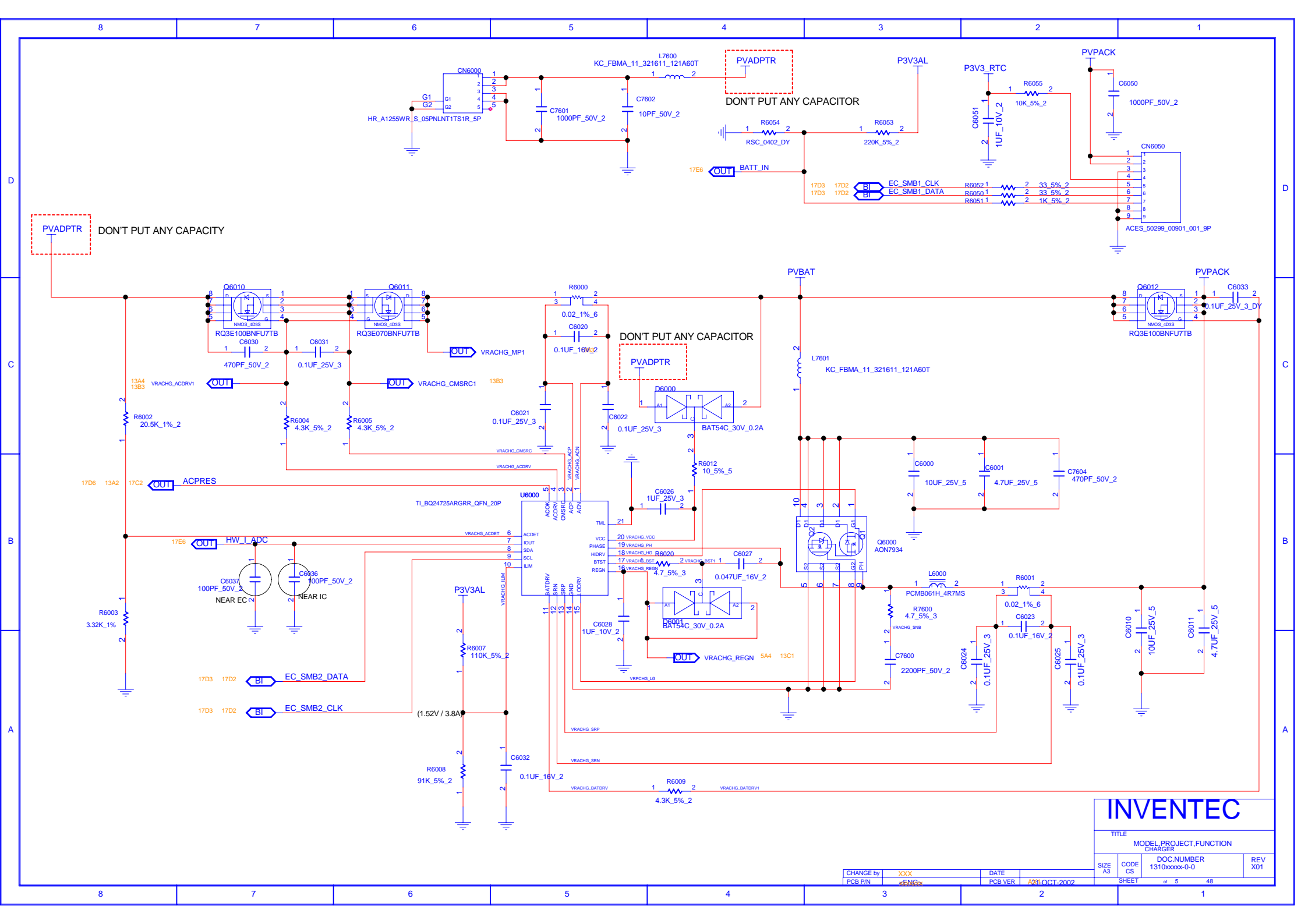
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET		2 of 48	

CHANGE by PCB P/N	XXX xxxxxx	DATE PCB VER	21-OCT-2002 AX1
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CHANGE by	XXX	DATE		MODEL	DOC NUMBER	REV
PCB P/N	ENG	PCB VER	2002	1310xxxx-0-0	X01	
SHEET		of 4		48		



INVENTEC

TITLE			
MODEL PROJECT, FUNCTION CHARGER			
SIZE A3		DOC. NUMBER 1310xxxxx-0-0	
CODE CS		REV X01	
SHEET		of 5 48	

CHANGE by	XXX	DATE	
PCB P/N	<ENG>	PCB VER	AXL OCT-2002

D

C

B

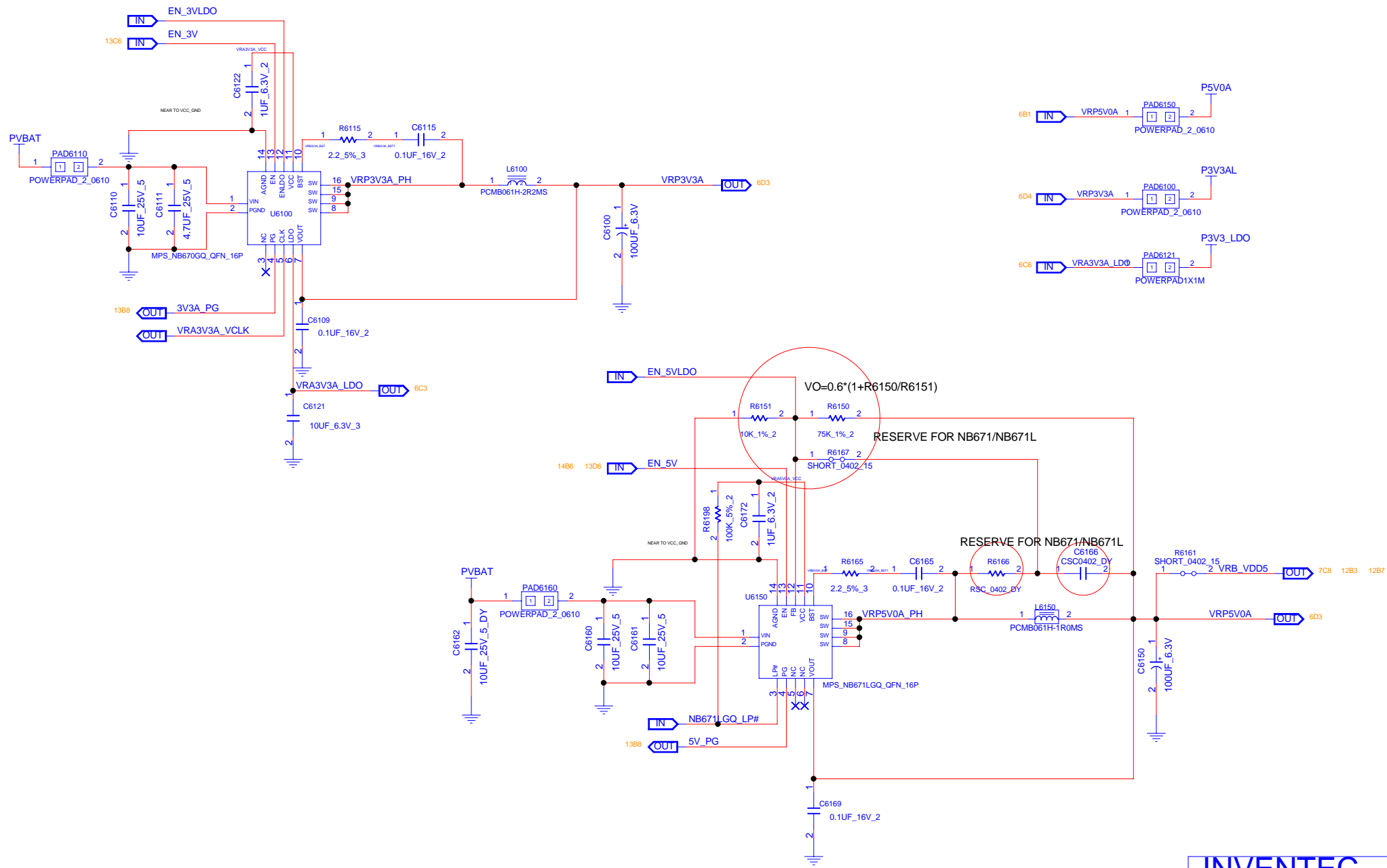
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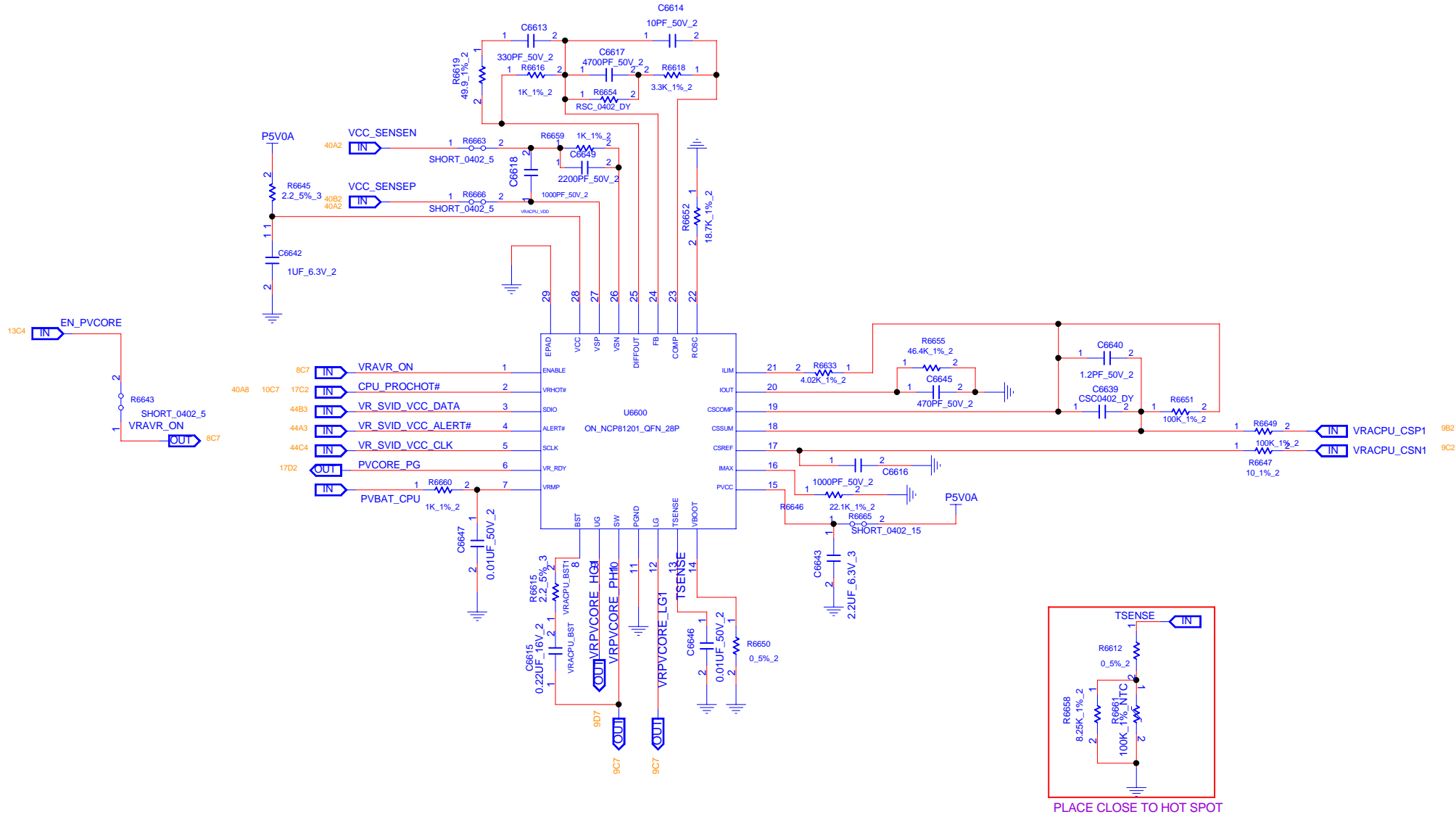
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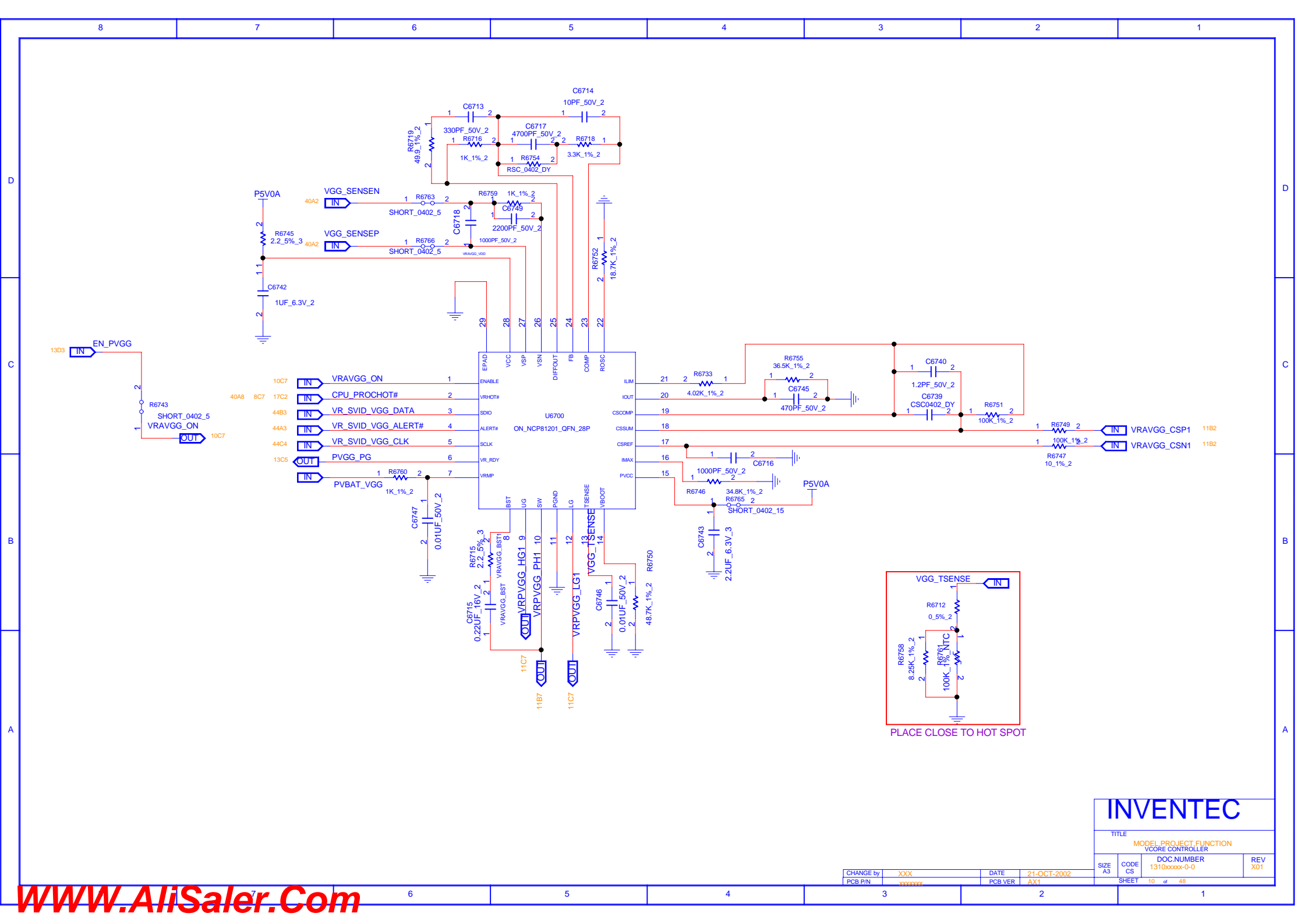
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3V/5V			
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A3	CS	1310xxxx-0-0	X01
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CHANGE by	XXX	DATE	
PCB P/N	<ENG>	PCB VER	2002



INVENTEC			
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MODEL PROJECT FUNCTION			
PIV065 POWER			
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SHEET 8 of 48			

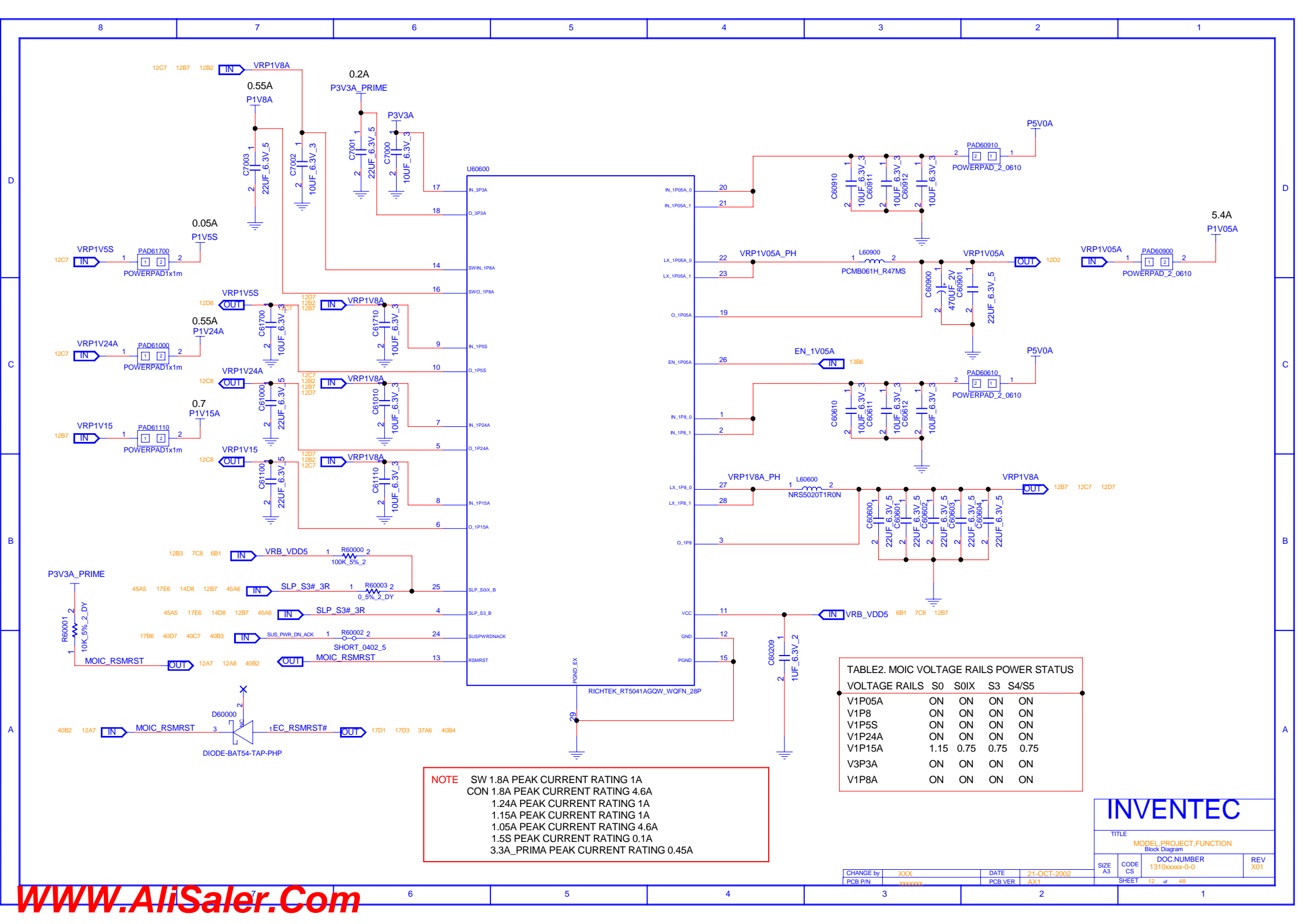
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	xxxxxx	PCB VER	AX1



INVENTEC

TITLE		
MODEL PROJECT FUNCTION		
VCORE CONTROLLER		
DOC NUMBER		
SIZE	CODE	1310xxxx-0-0
A3	CS	
SHEET 10 of 48		

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NOTE SW 1.8A PEAK CURRENT RATING 1A
CON 1.8A PEAK CURRENT RATING 4.6A
1.24A PEAK CURRENT RATING 1A
1.15A PEAK CURRENT RATING 1A
1.05A PEAK CURRENT RATING 4.6A
1.5S PEAK CURRENT RATING 0.1A
3.3A_PRIMA PEAK CURRENT RATING 0.45A

TABLE2. MOIC VOLTAGE RAILS POWER STATUS				
VOLTAGE RAILS	S0	S0IX	S3	S4/S5
V1P05A	ON	ON	ON	ON
V1P8	ON	ON	ON	ON
V1P5S	ON	ON	ON	ON
V1P24A	ON	ON	ON	ON
V1P15A	1.15	0.75	0.75	0.75
V3P3A	ON	ON	ON	ON
V1P8A	ON	ON	ON	ON

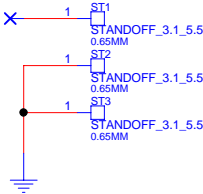
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MODEL PROJECT,FUNCTION Block Diagram		
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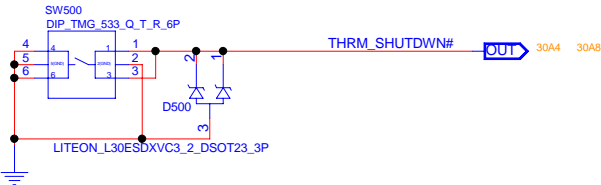
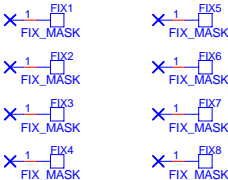
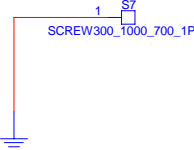
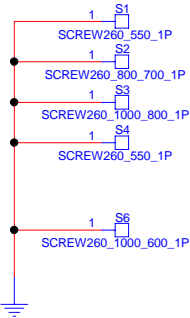
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	xxxxxx	PCB VER	AX1

REFERENCE 0~49(PCB SCREW)

CPU



PCB



INVENTEC

TITLE MODEL PROJECT FUNCTION Block Diagram

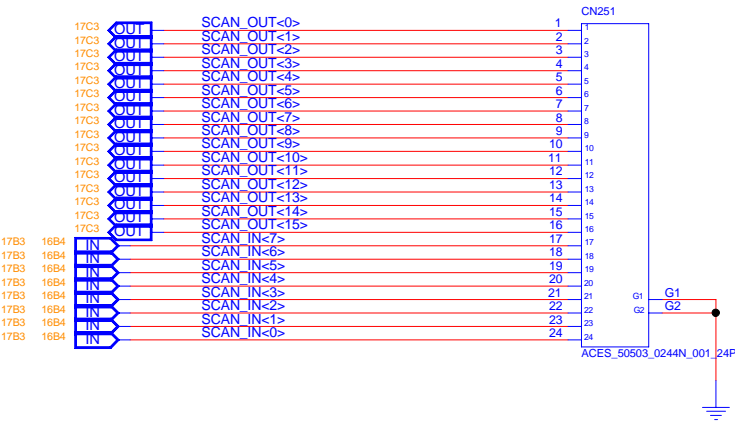
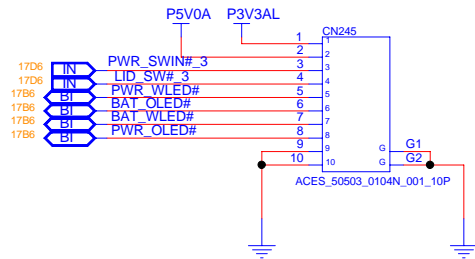
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CHANGE by XXX DATE 21-OCT-2002 PCB P/N xxxxxx PCB VER AX1

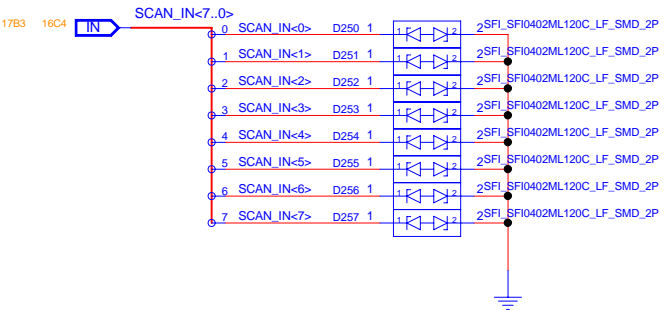
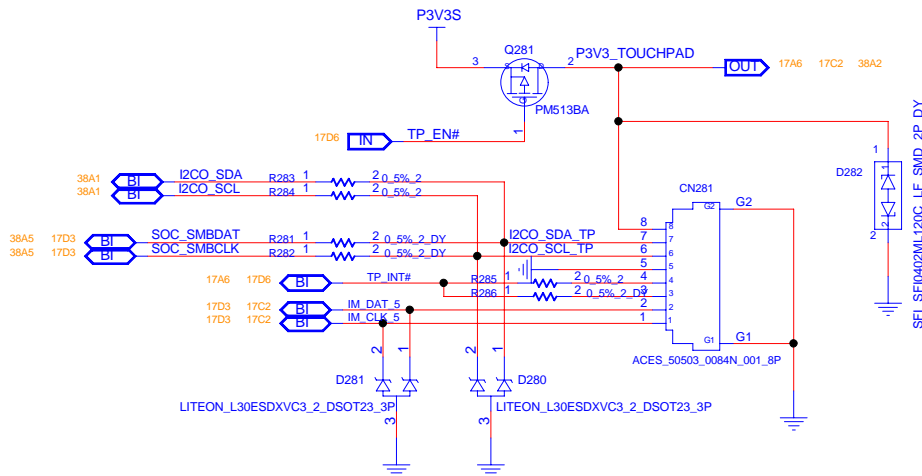
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REFERENCE 250~299(KB/TP CONN)

KEYBOARD CONN



TOUCHPAD CONN (CLICK PAD)



INVENTEC

TITLE MODEL PROJECT FUNCTION

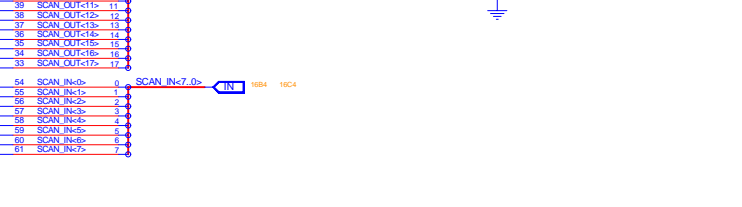
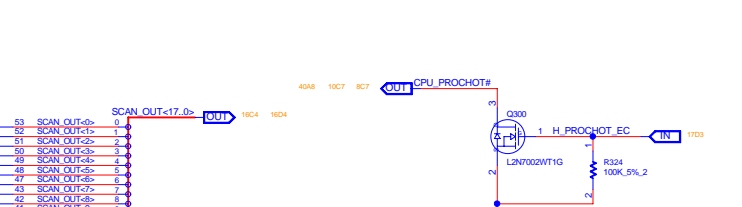
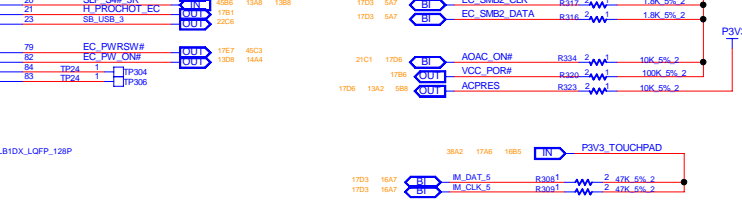
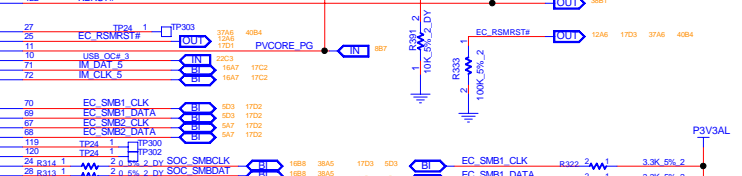
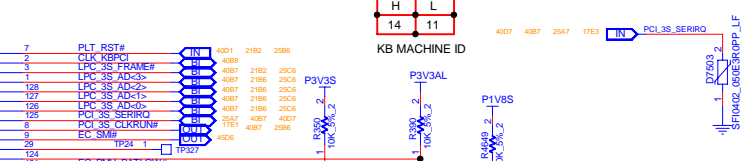
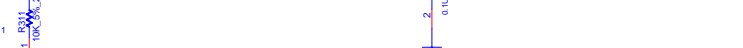
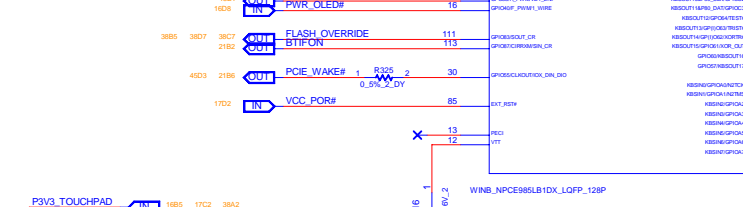
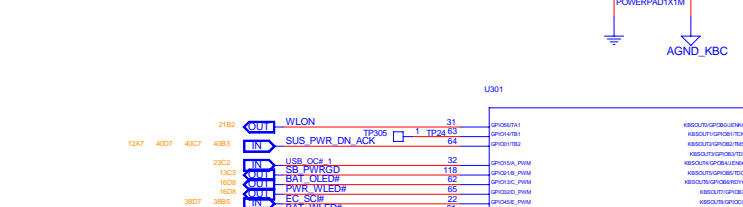
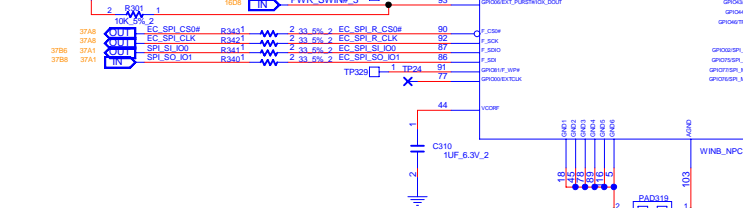
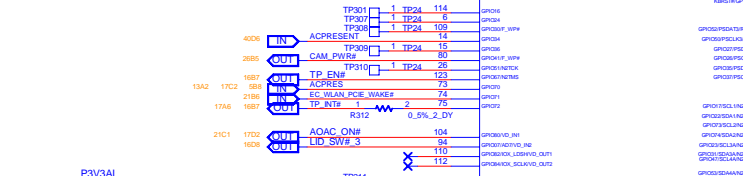
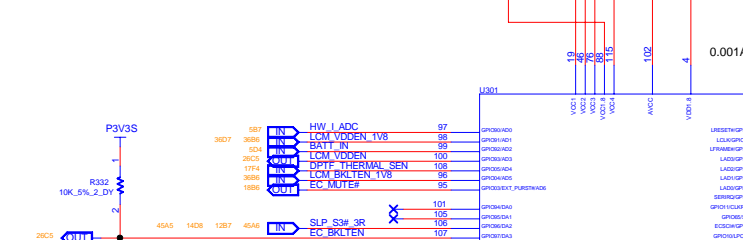
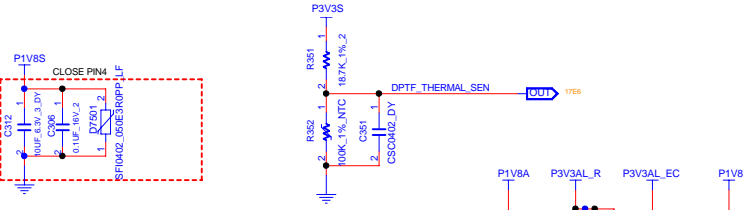
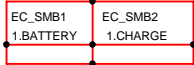
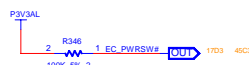
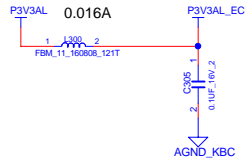
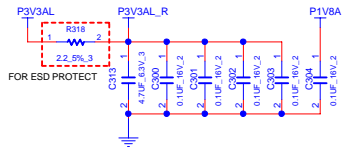
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REV X01

CHANGE by XXX PCB P/N xxxxxx DATE 21-OCT-2002 PCB VER AX1

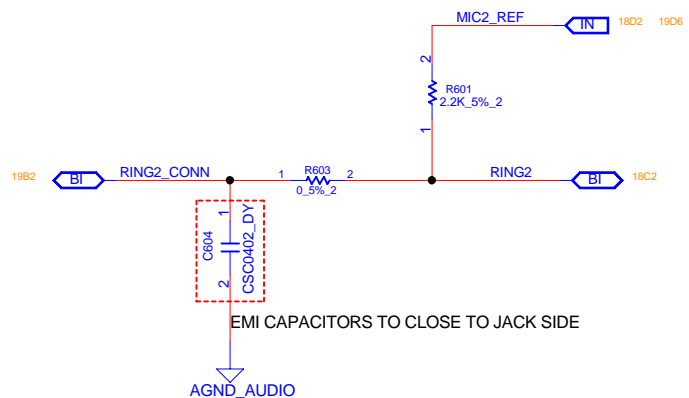
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REFERENCE 300~389(KBC)



INVENTEC

MODEL/PROJECT/FUNCTION	EC
DOC NUMBER	REV
1310XXXXXX-02	X01

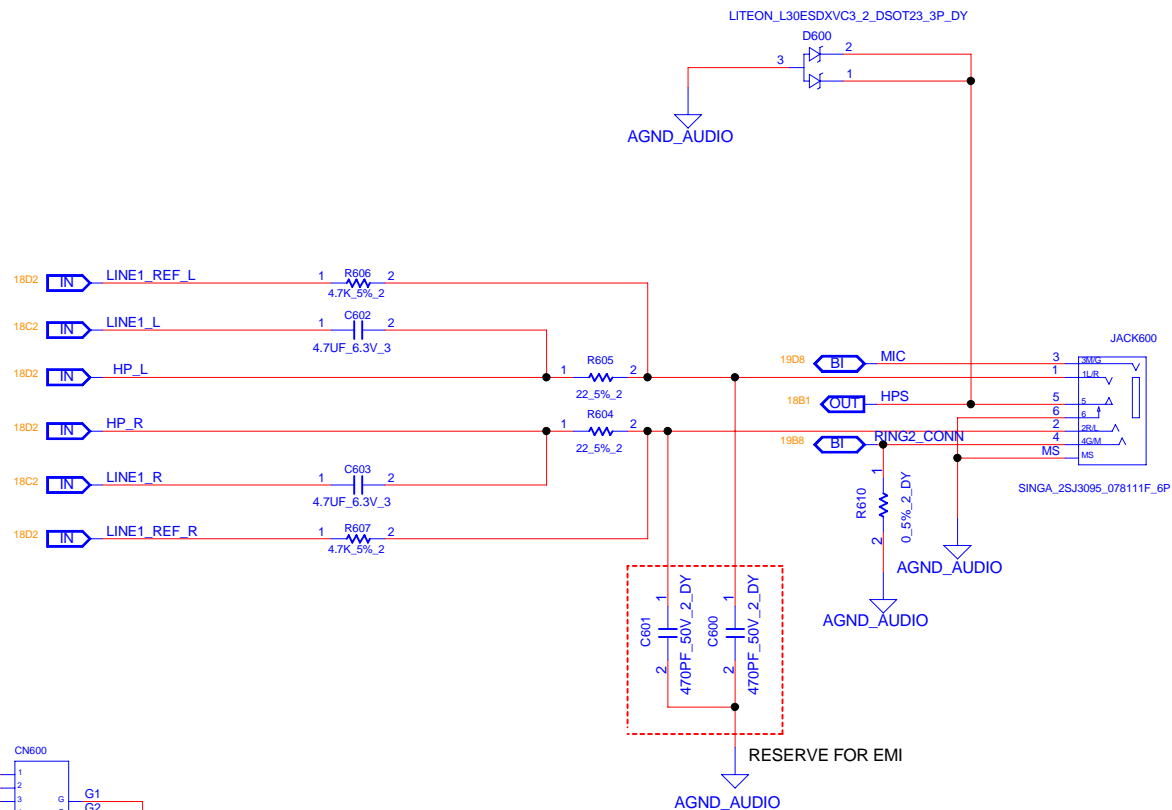


INTERNAL SPEAKERS

NOTE: SPK TRACE SHOULD 30-40 MILS WIDTH

The diagram shows a PCB layout for speaker traces. On the left, a 4-pin connector is labeled with pin numbers 1867, 18C7, 18C7, and 18C7. The pins are labeled: SPK OUT R R P, SPK OUT R R N, SPK OUT R L N, and SPK OUT R L P. A red dashed box contains five decoupling capacitors: C611, C610, C609, C608, and C607, each with a value of 1 and a tolerance of 2. These capacitors are connected to the speaker traces. A component labeled CN600 is shown on the right, with pins 1, 2, 3, and 4. It is connected to G1 and G2. A label LCN_AWM10_0429980_0004_4P is also present. A note at the bottom states: RESERVE FOR EMI, PLACEMENT NEAR CONNECTOR.

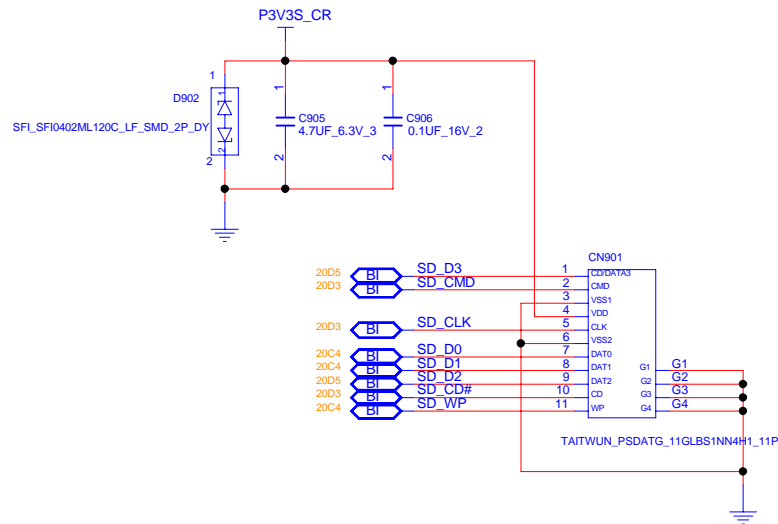
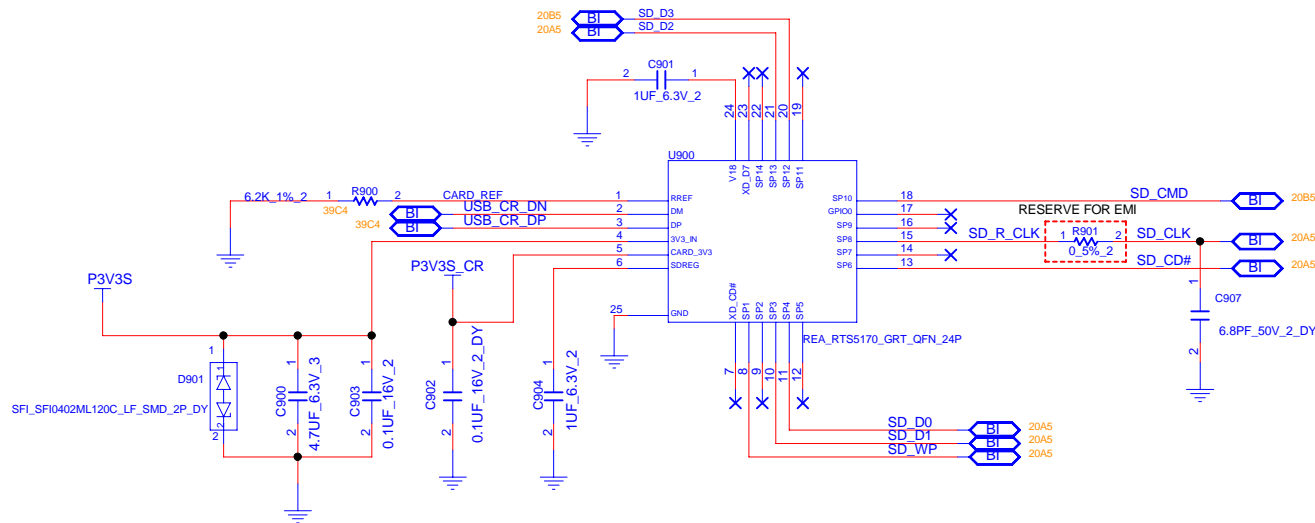
RESERVE FOR EMI, PLACEMENT NEAR CONNECTOR



INVENTEC

TITLE		
MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
SHEET 19 of 48		

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PCB P/N	xxxxxxx	PCB VER	AX1



INVENTEC

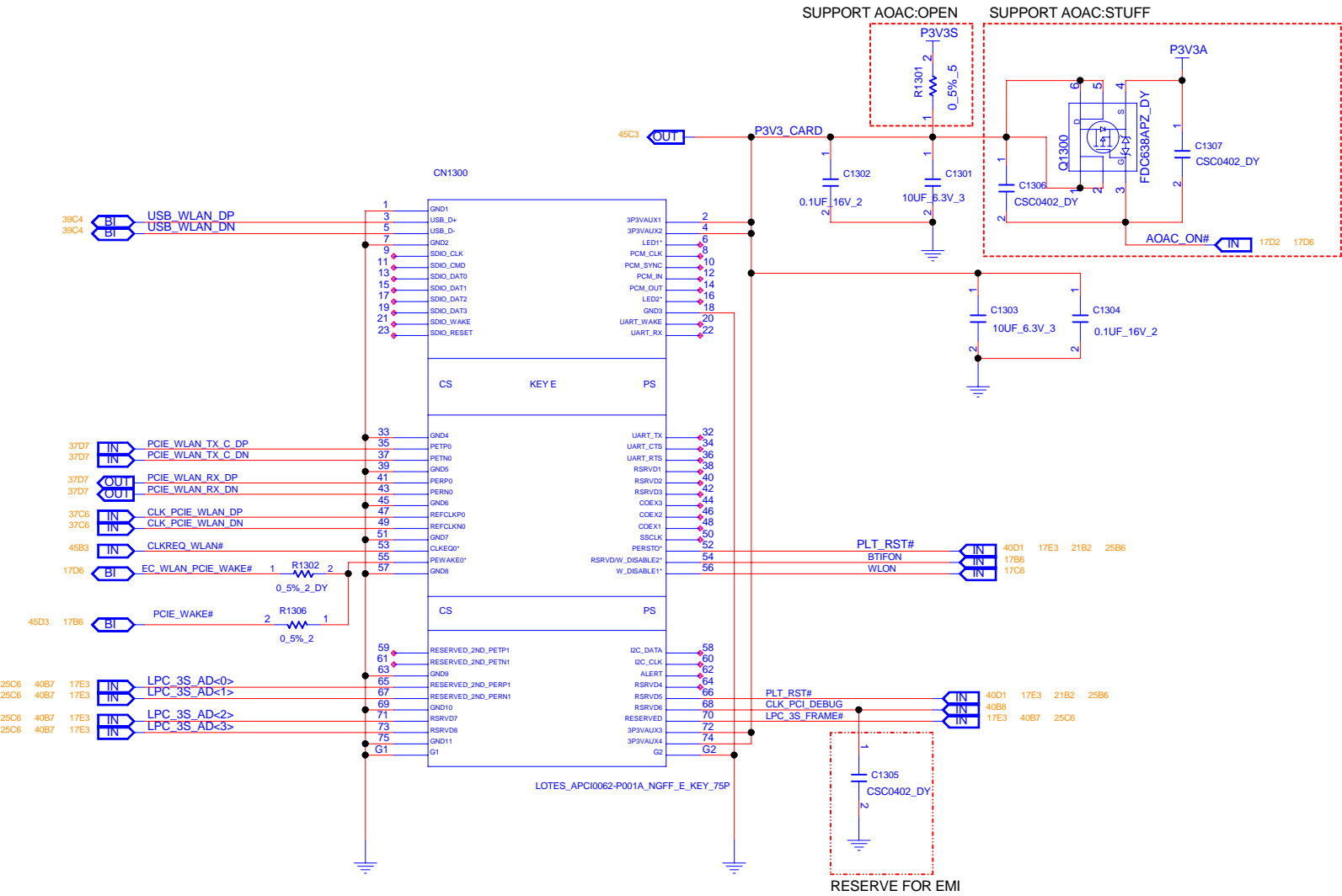
TITLE
MODEL PROJECT FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 20 of 48			

CHANGE by PCB P/N	XXX xxxxxx	DATE PCB VER	21-OCT-2002 AX1
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REFERENCE 1300~1349(WLAN)

WIFI AND DEBUG CARD CO-LAYOUT CONNECTOR



INVENTEC

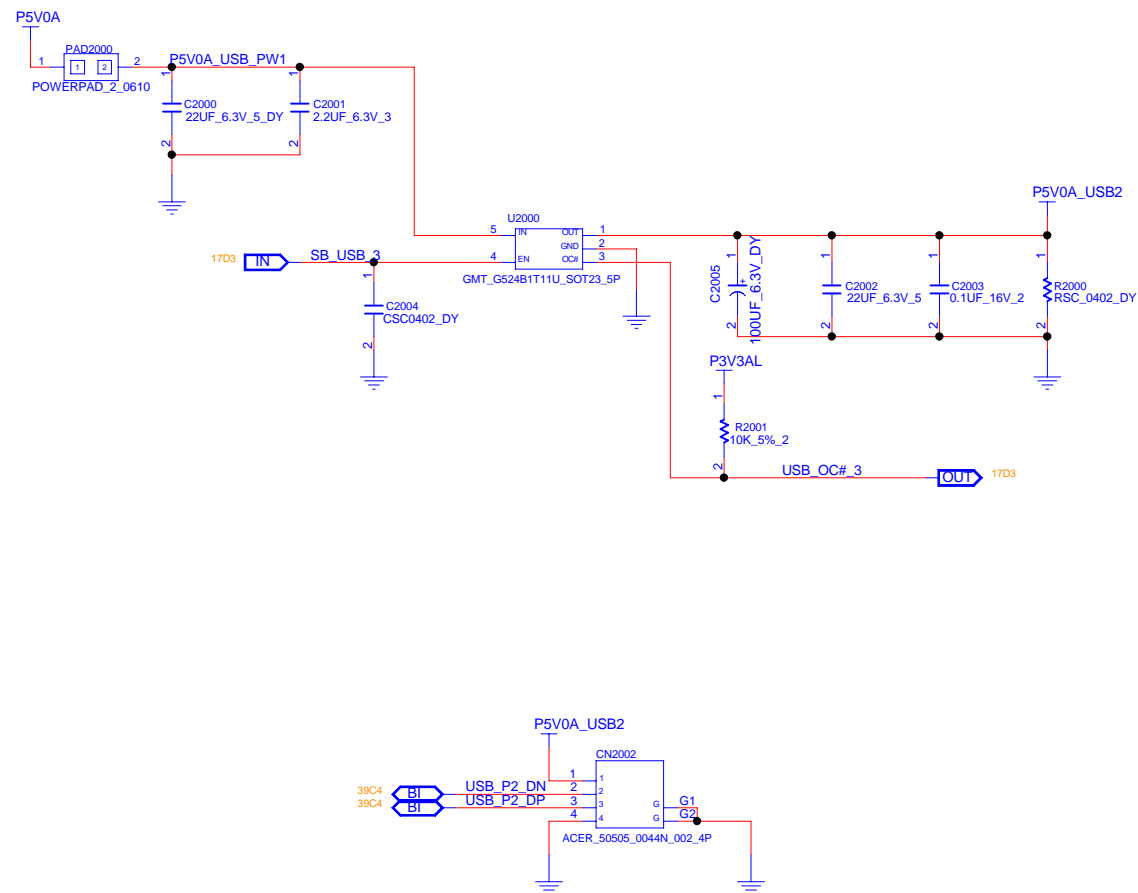
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CHANGE by XXX DATE 21-OCT-2002
PCB P/N xxxxxx PCB VER AX1

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REFERENCE 2000~2099(USB)



INVENTEC

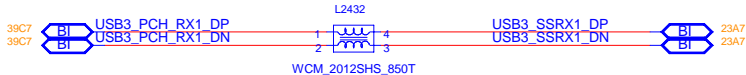
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SIZE	CODE	DOC NUMBER	REV
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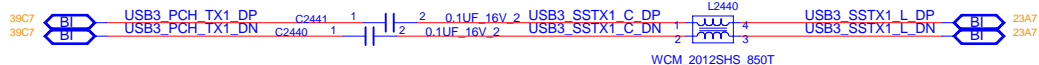
CHANGE by	XXX	DATE	21-OCT-2002
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REFERENCE 2400~2499(USB3.0)

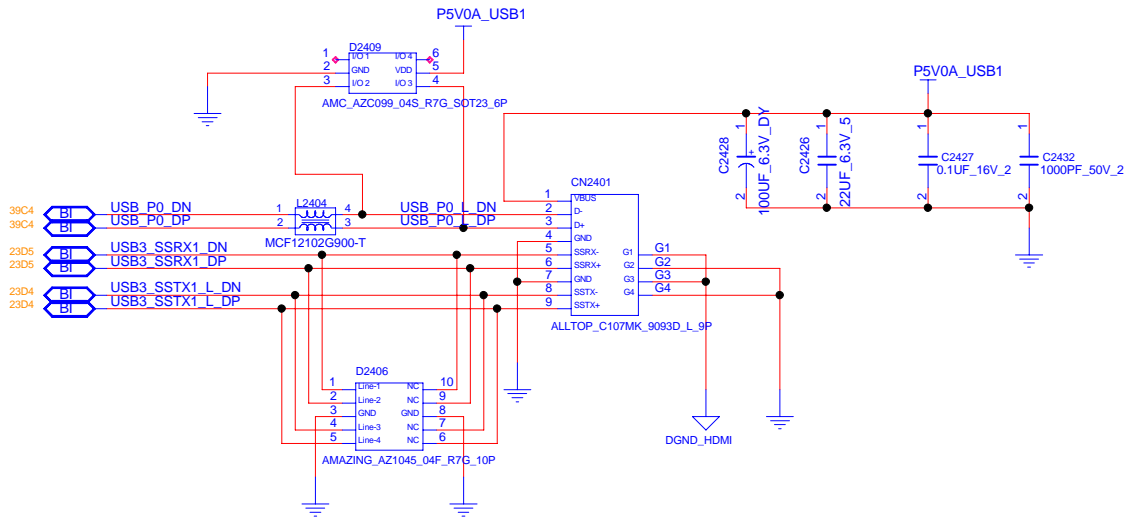
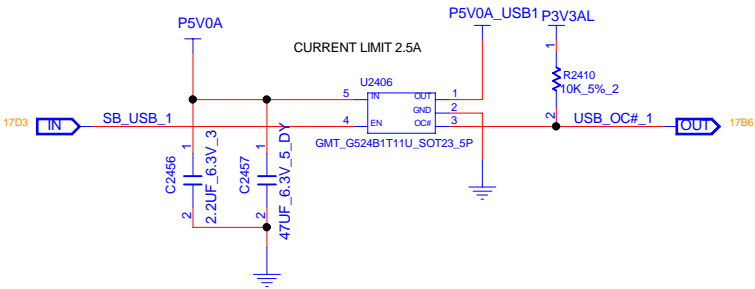
USB3.0 FROM PCH



USB3.0 FROM PCH



USB 3.0 CONNECTOR



INVENTEC

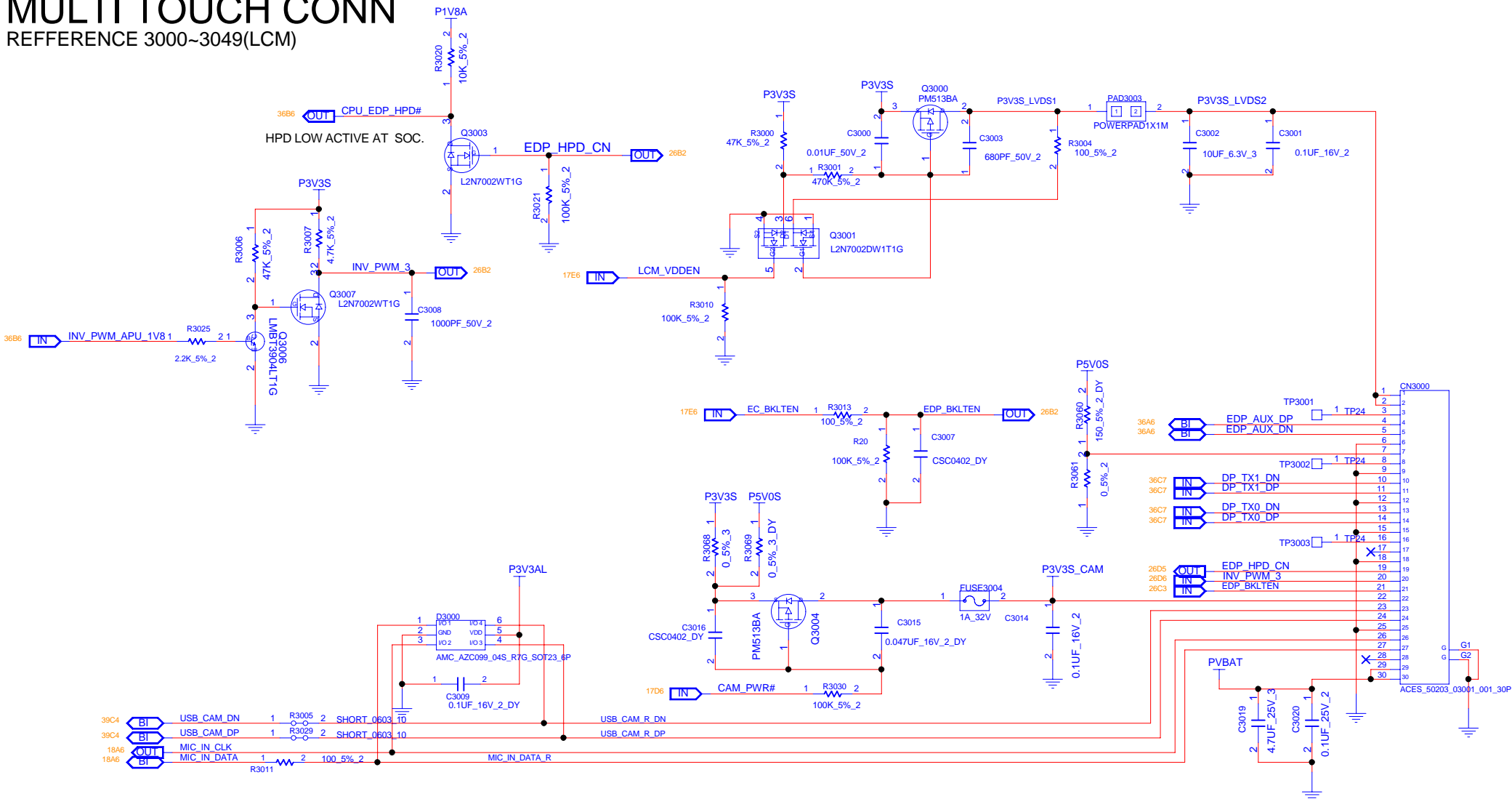
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MODEL PROJECT FUNCTION
Block Diagram

SIZE CODE DOC NUMBER REV
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CHANGE by XXX DATE 21-OCT-2002
PCB P/N xxxxxx PCB VER AX1

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REFERENCE 3000~3049(LCM)



TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

		DOC.NUMBER
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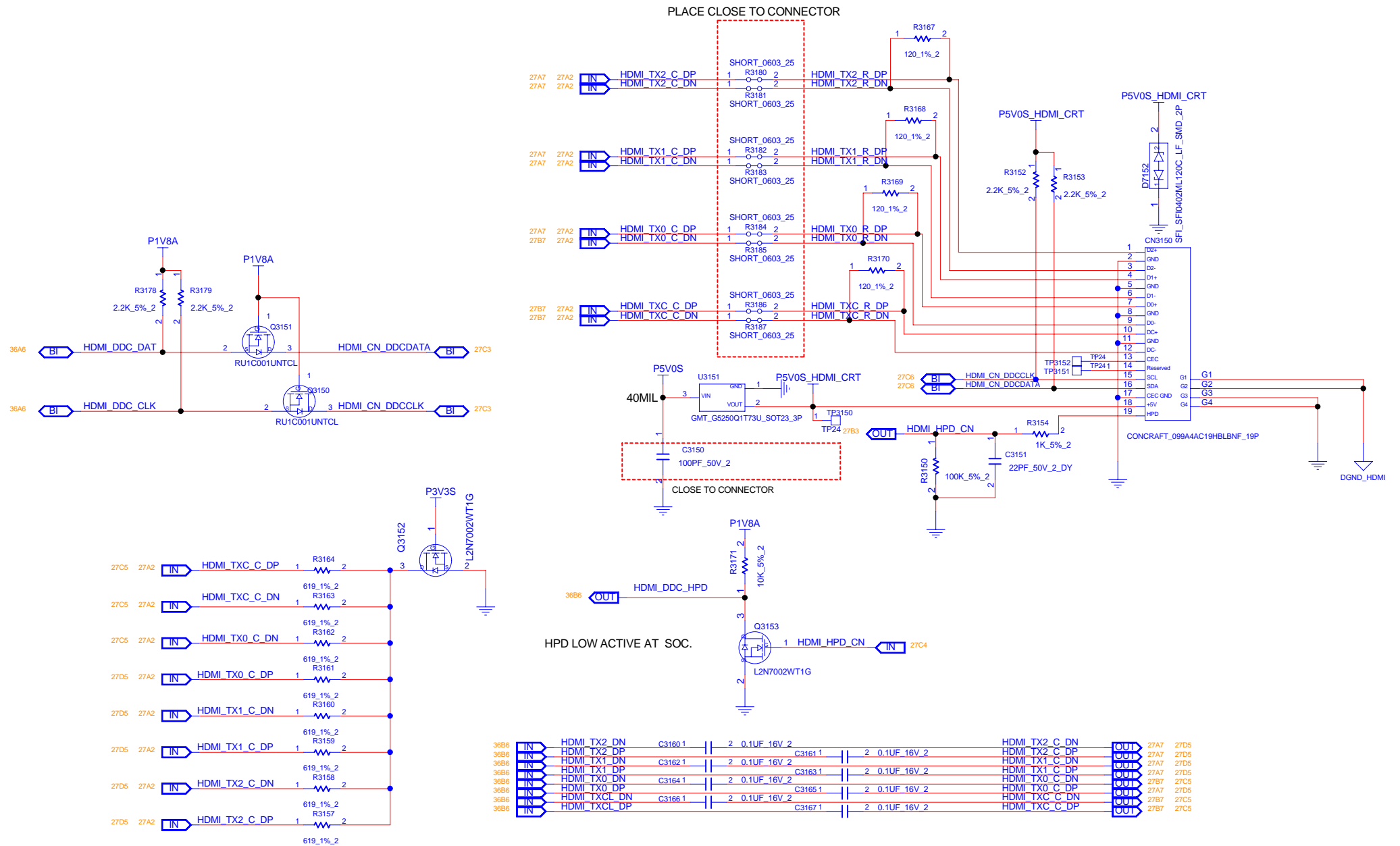
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	xxxxxxx	PCB VER	AX1

3	2
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REFERENCE 3150~3199(HDMI)



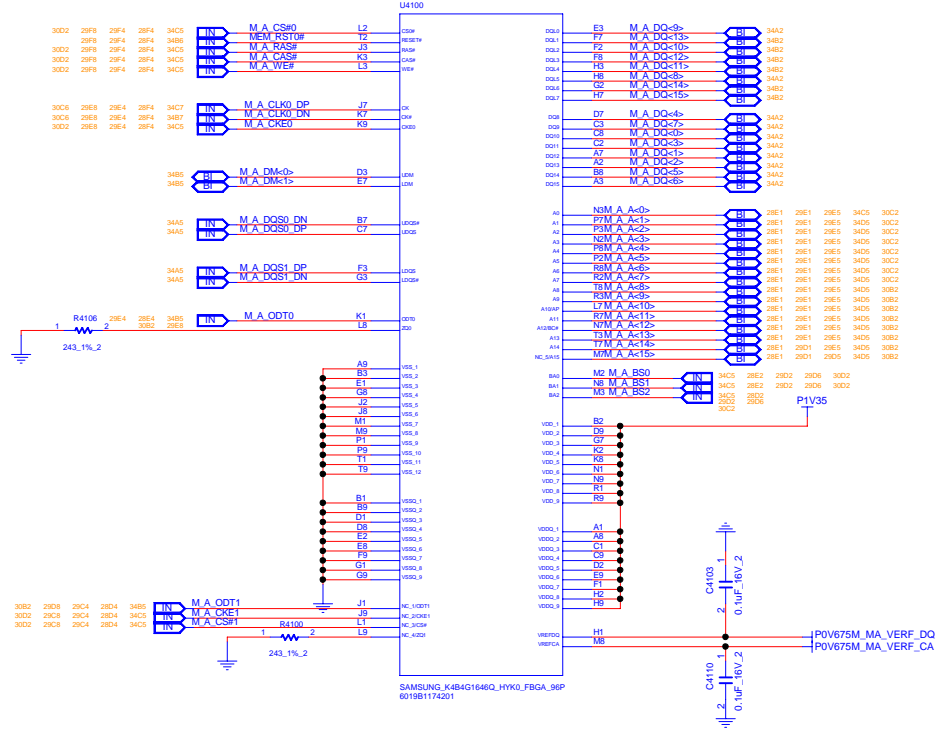
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SHEET of 27 48			

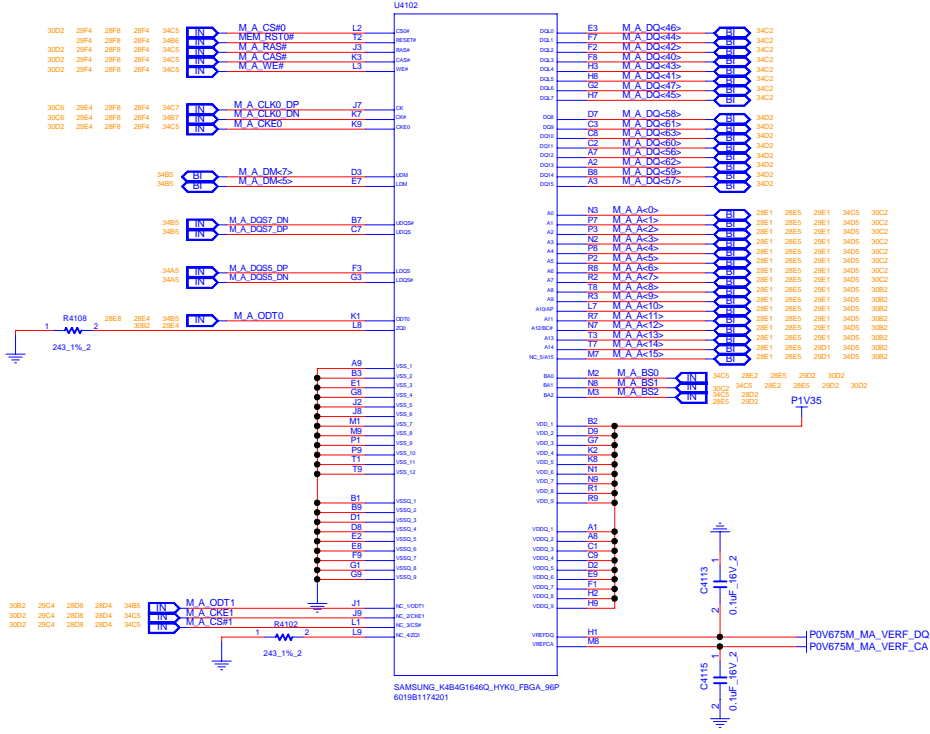
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PCB P/N	ENG	PCB VER	AX1-OCT-2002

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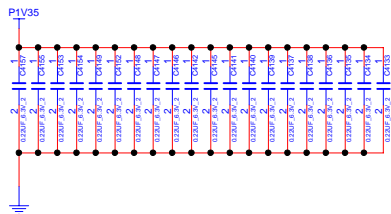
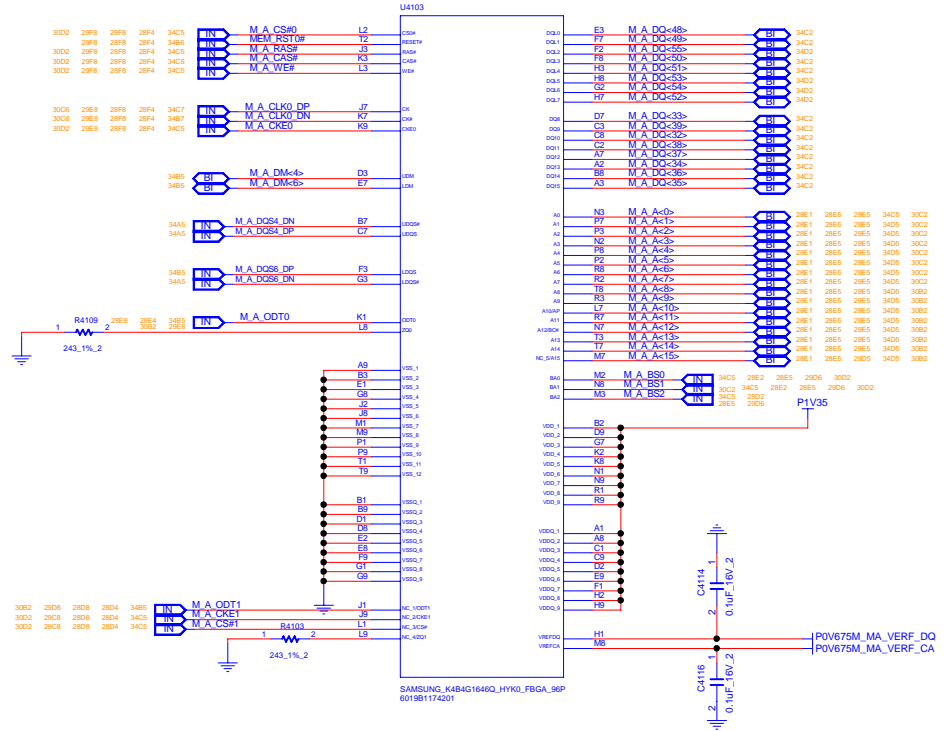
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DDR3L_2



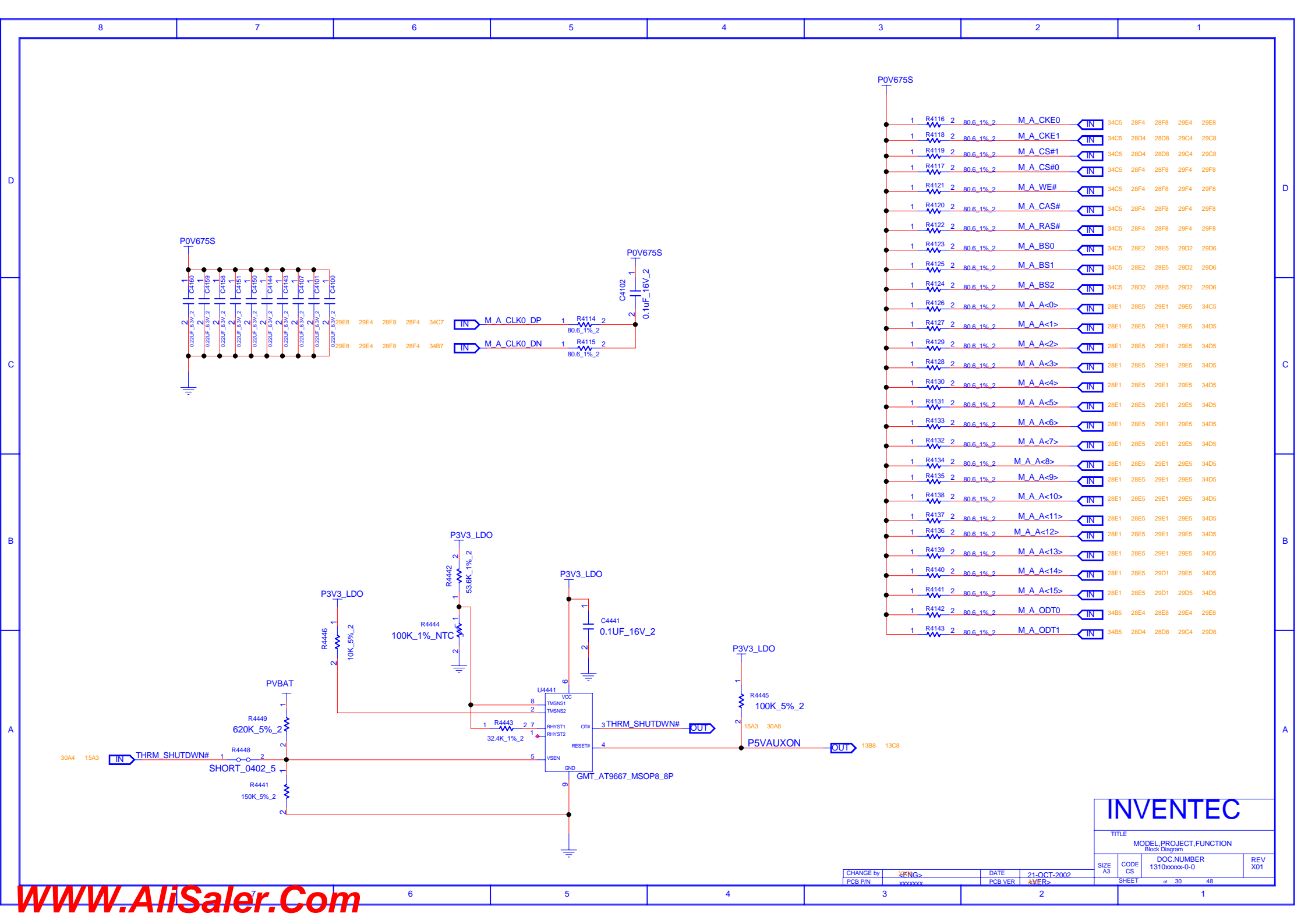
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INVENTEC

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SHEET	#	29	38

CHANGES	DATE	BY	APP
PCB PIN	21-OCT-2002	AMER	



INVENTEC

TITLE MODEL PROJECT FUNCTION

Block Diagram

DOC NUMBER 1310xxxxx-0-0

REV X01

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PCB P/N xxxxxx PCB VER AVER>

F



F



F



A

CHANGE by	xxx	DATE	21-OCT-2002
PCB P/N	xxxxxxxx	PCB VER	AX1

D

C

B

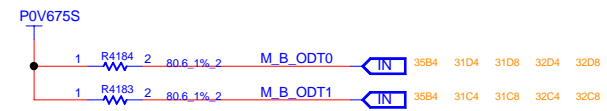
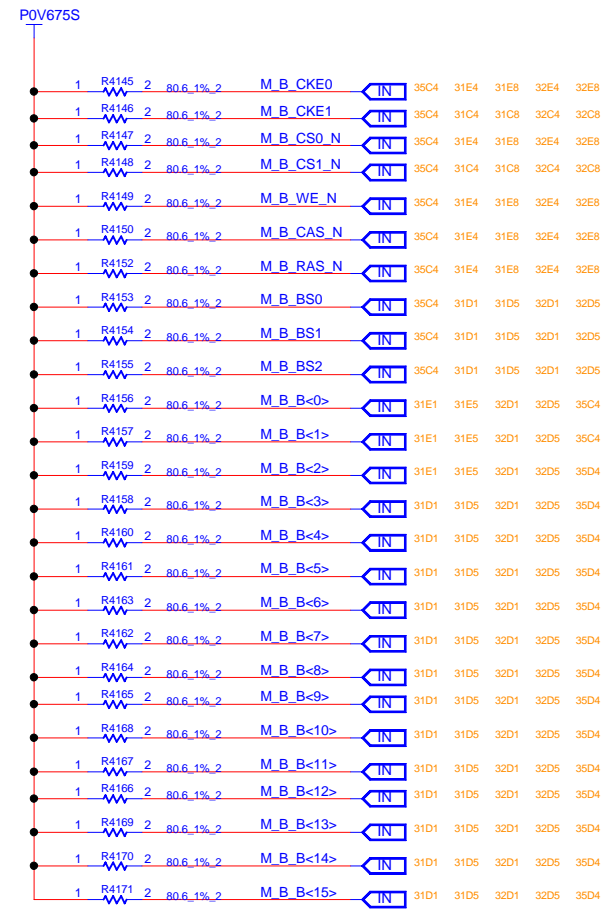
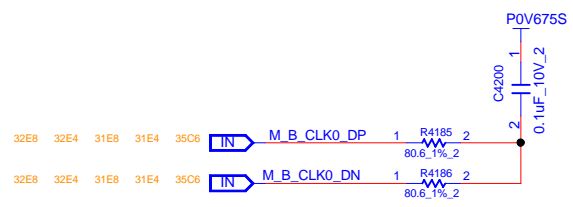
A

D

C

B

A



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

DOC NUMBER
1310xxxx-0-0

REV
X01

SIZE
A3

CODE
CS

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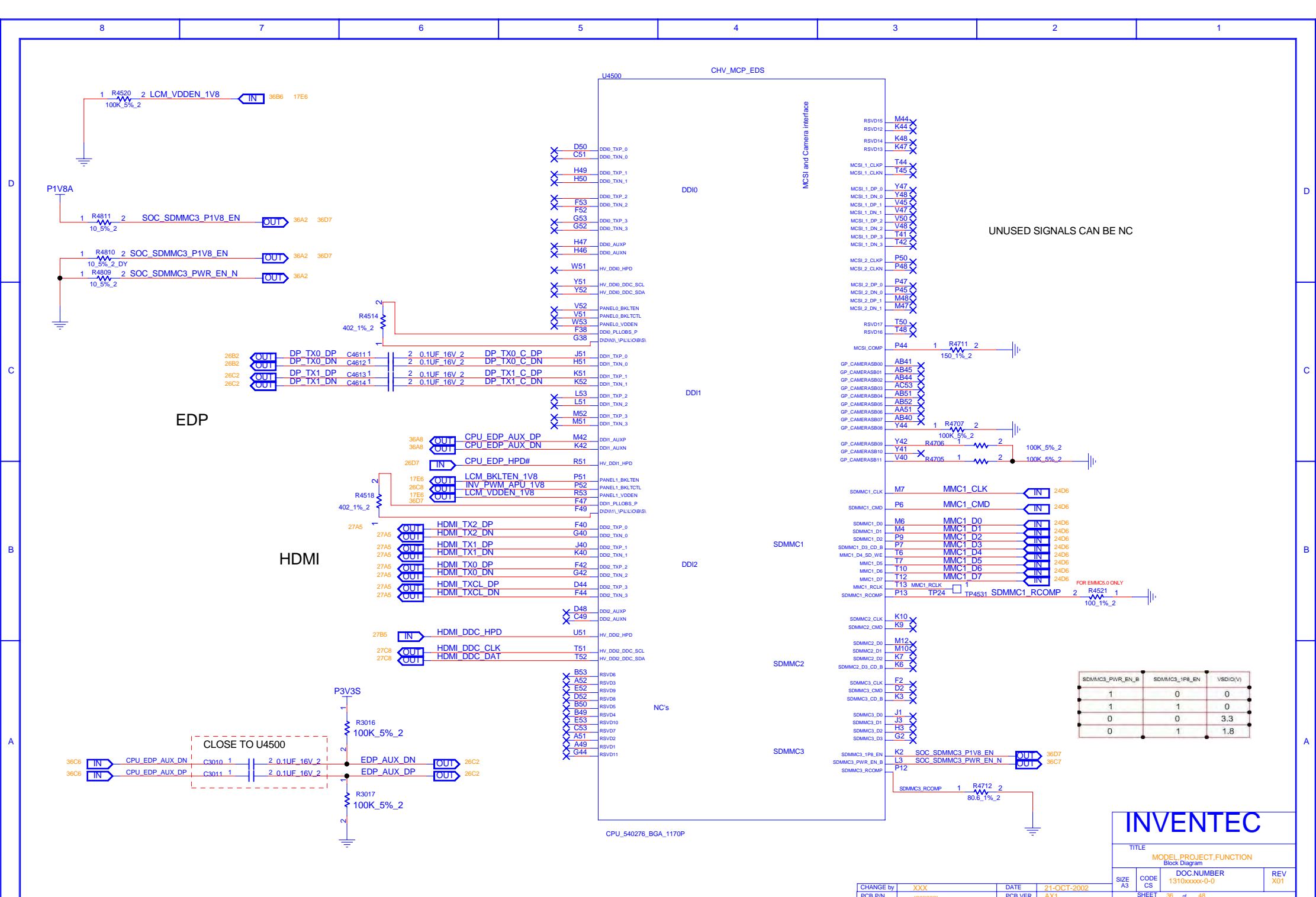
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PCB P/N	xxxxxx	PCB VER	AX1

D



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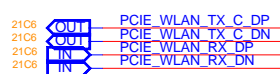


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TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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PCB P/N	xxxxxx	PCB VER	AX1

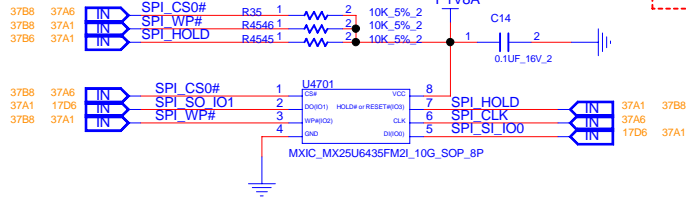
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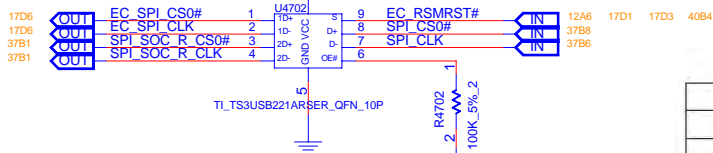
P1V8A

CLK PCIE WLAN DP
CLK PCIE WLAN DNPCIE_OBSP
PCIE_OBSN

SPI FLASH



P3V3_LDO



TRUTH TABLE

S	OE	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

INVENTEC

TITLE

MODEL PROJECT FUNCTION

Block Diagram

SIZE

CODE

CS

DOC NUMBER

REV

SHEET

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of

48

X01

CHANGE by
PCB P/N

XXX

XXXXXX

DATE
PCB VER

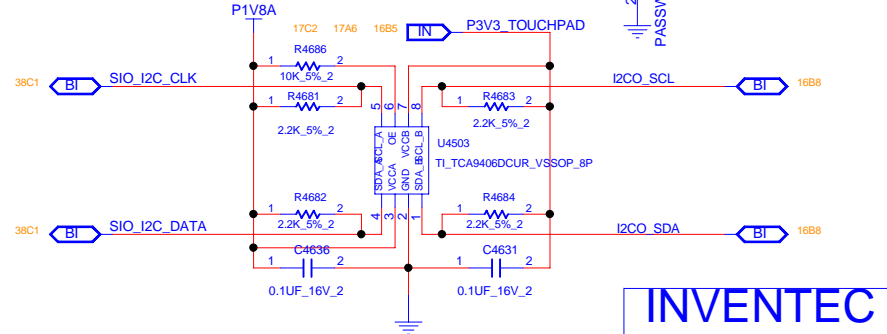
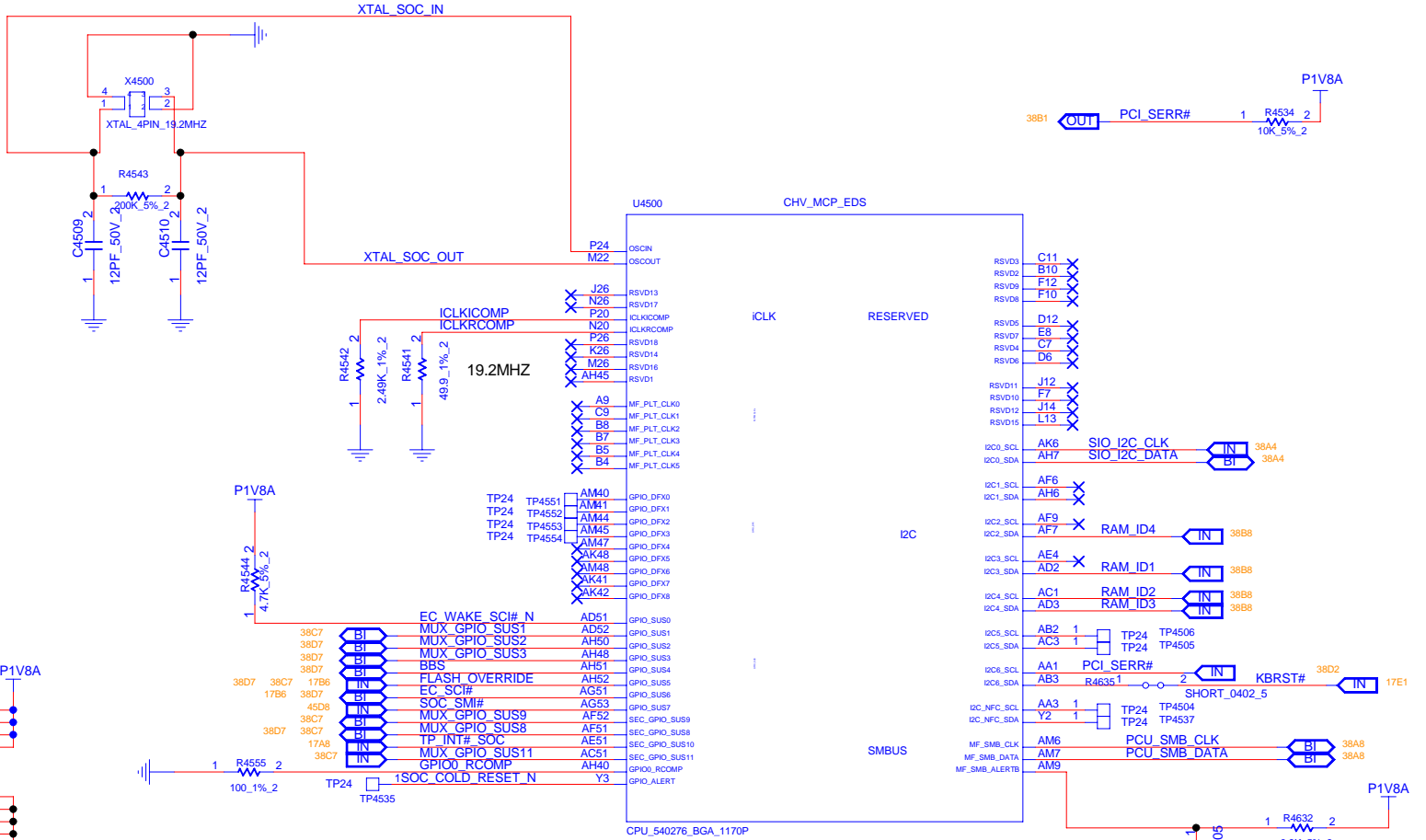
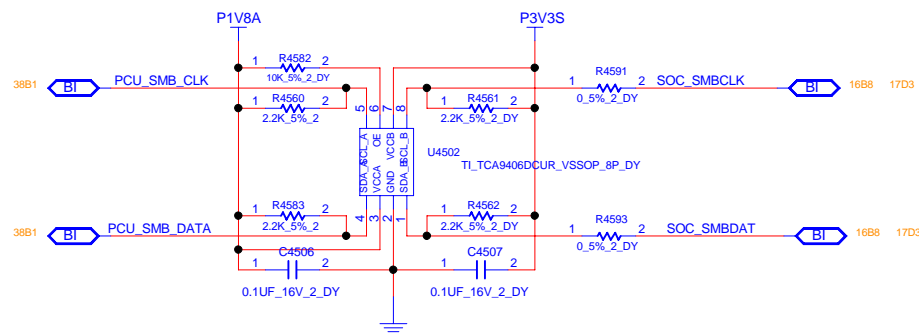
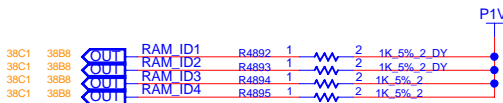
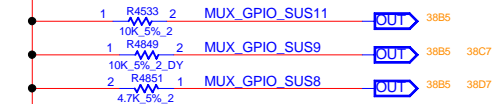
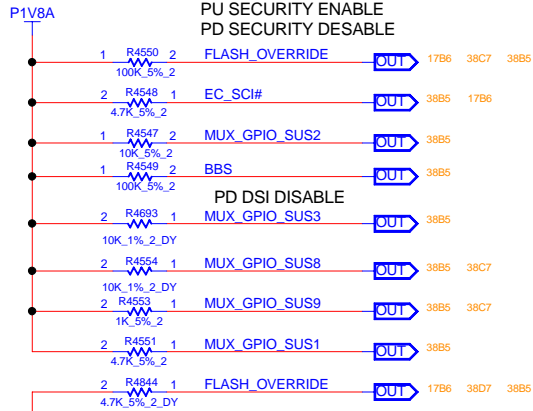
21-OCT-2002

AX1

STRAP PIN

PLEASE REFERENCE TO CRB PAGE23

PU SECURITY ENABLE
PD SECURITY DESABLE

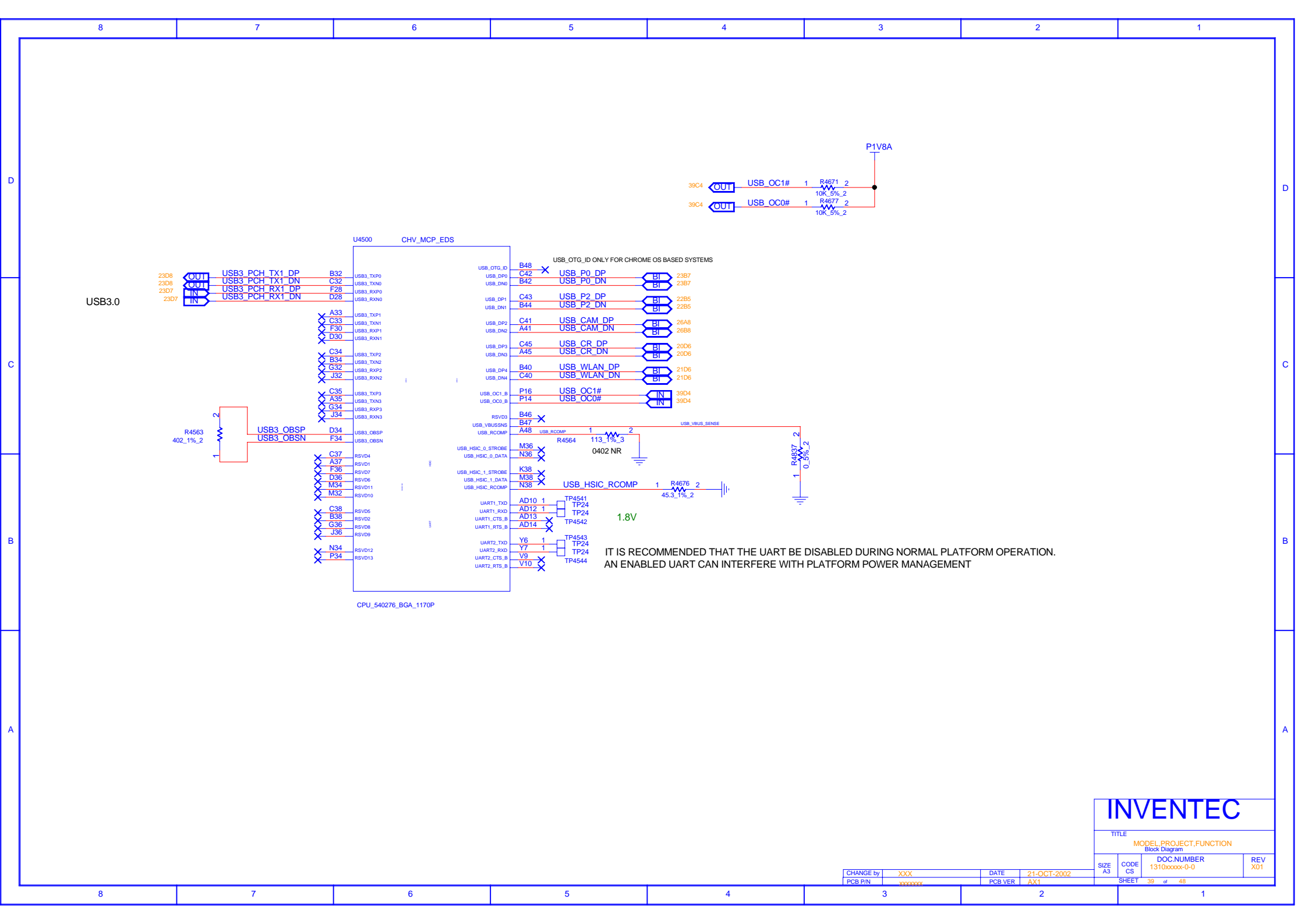


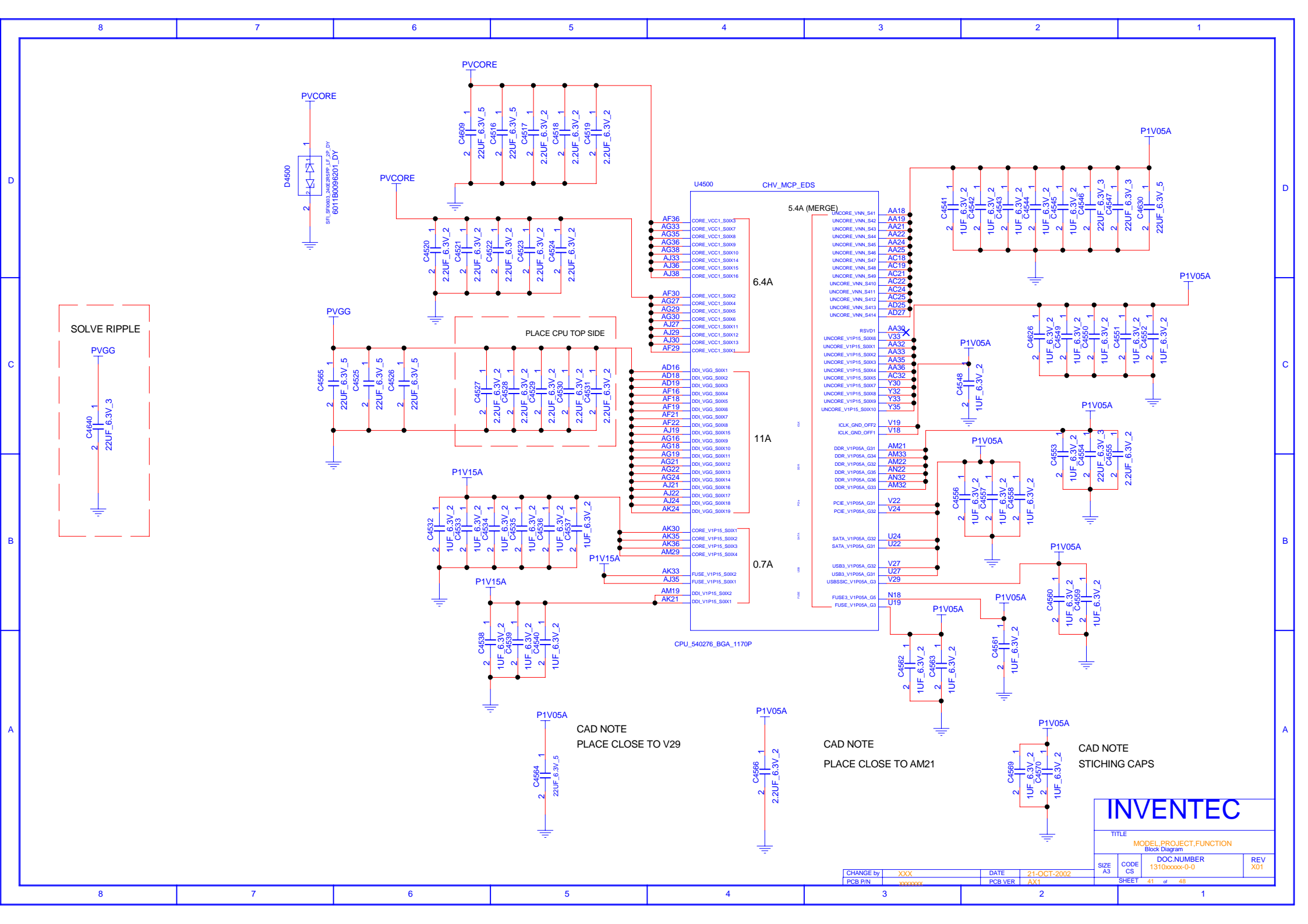
INVENTEC

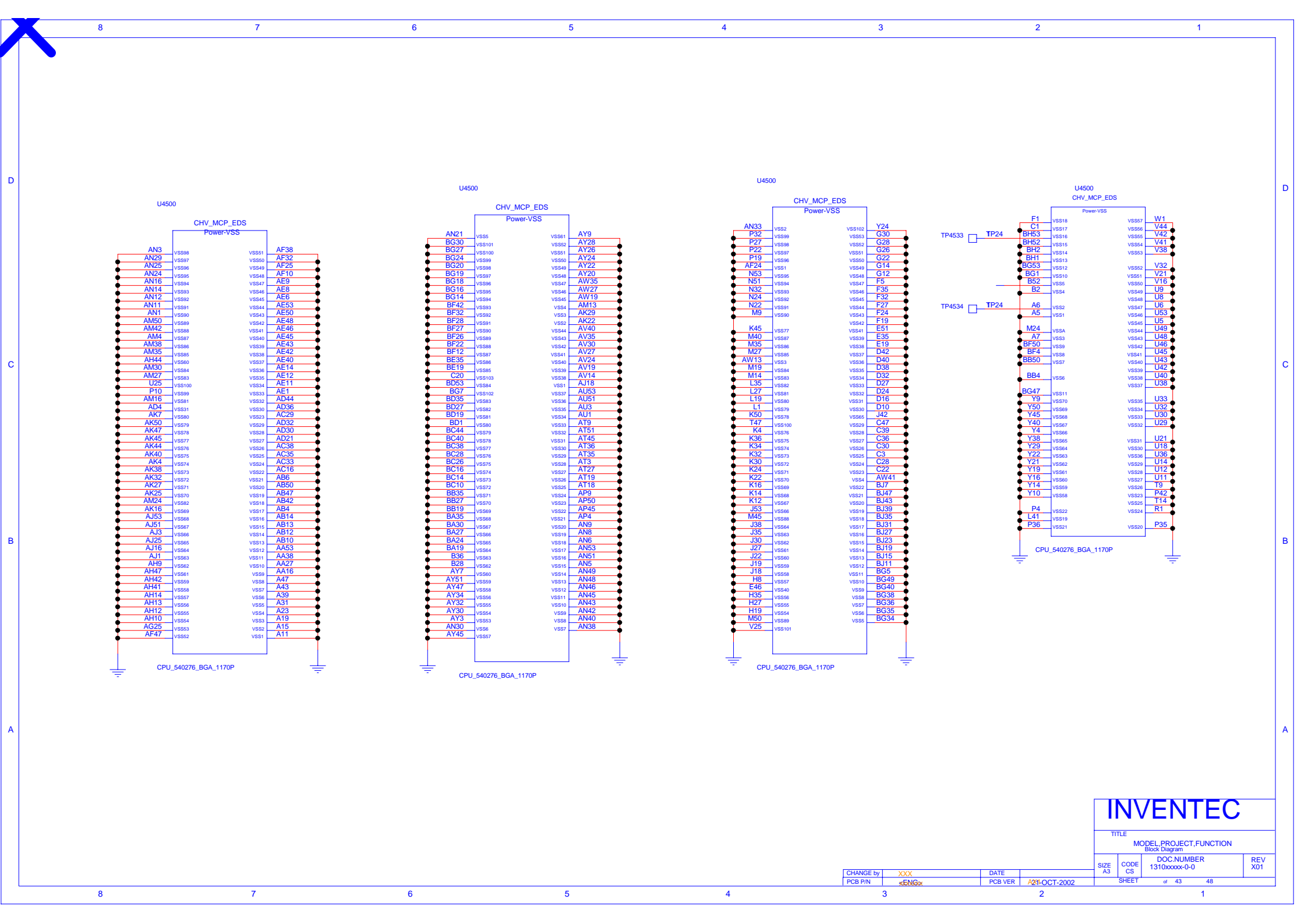
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
DOC NUMBER			
1310xxxxx-0-0			
REV X01			
SIZE	CODE	SHEET	
A3	CS	of 38 48	

CHANGE by	XXX	DATE	
PCB P/N	ENG	PCB VER	

DATE	2002
PCB VER	



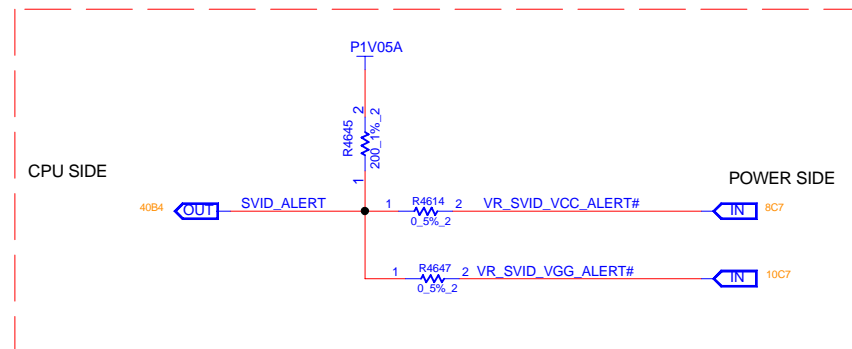
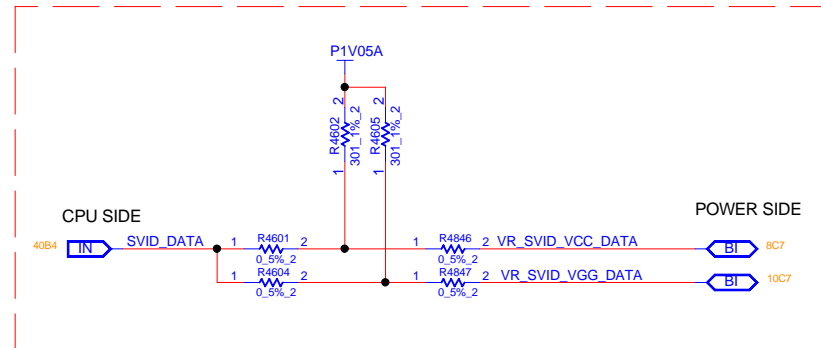
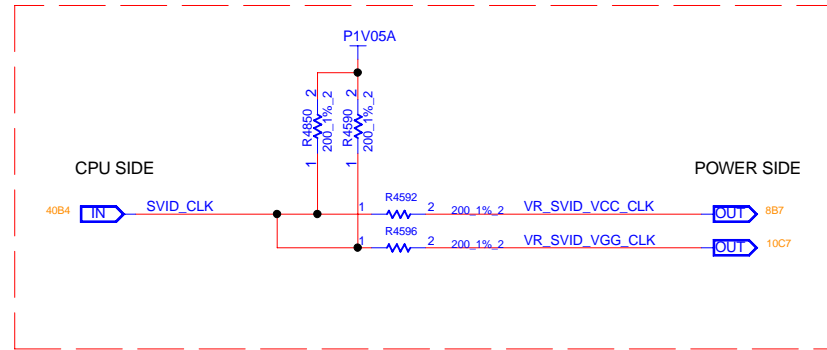




CHANGE by	XXX	DATE	
PCB P/N	ENG	PCB VER	

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
DOC NUMBER			
1310xxxxx-0-0			
SIZE	CODE	REV	
A3	CS	X01	
SHEET		of 43	48

SVID



INVENTEC

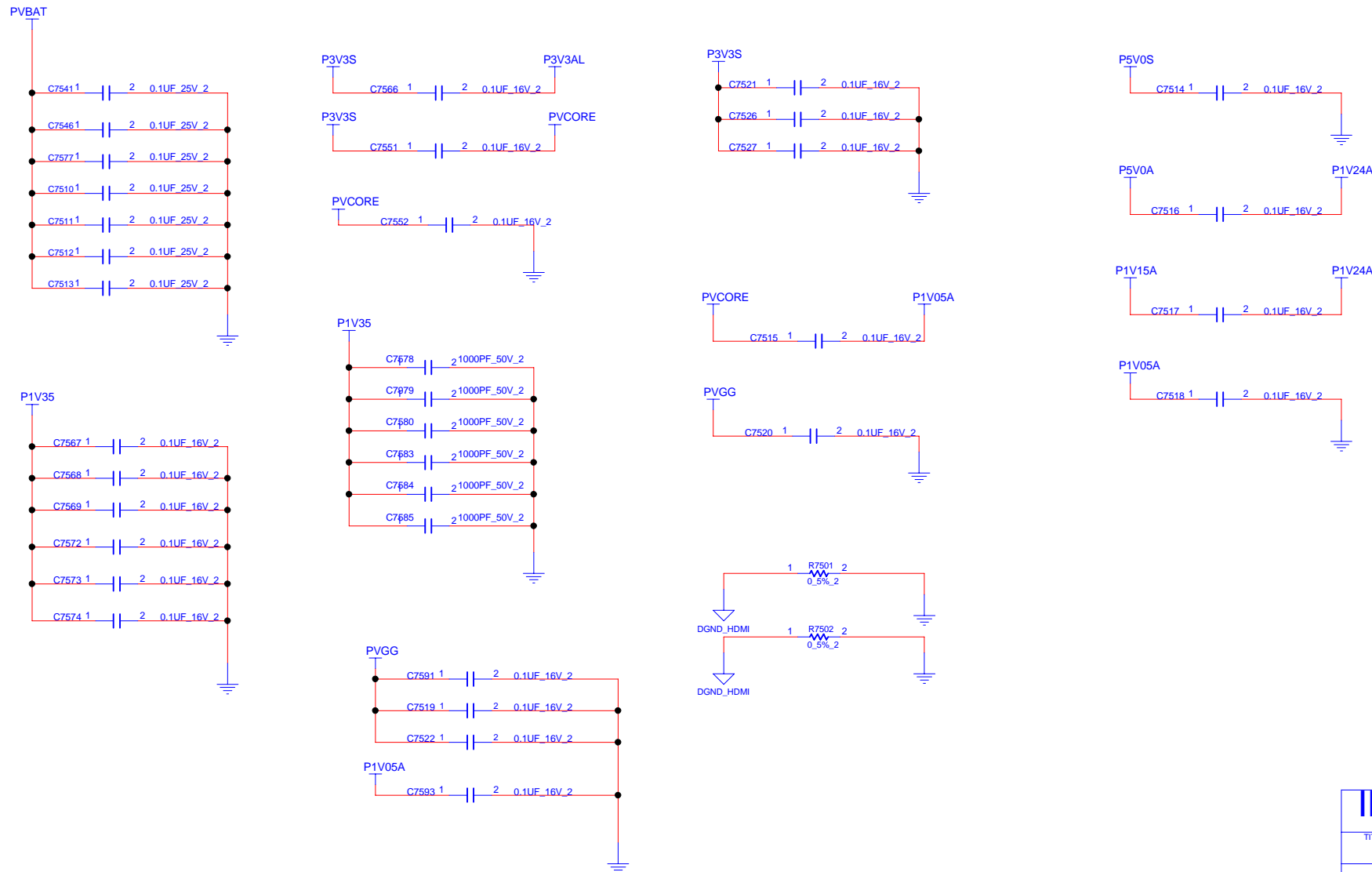
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by	DATE
PCB P/N XXX	21-OCT-2002
PCB VER yyyyyy	AX1

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EMI



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		46 of 48	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	xxxxxx	PCB VER	AX1

D

D

C

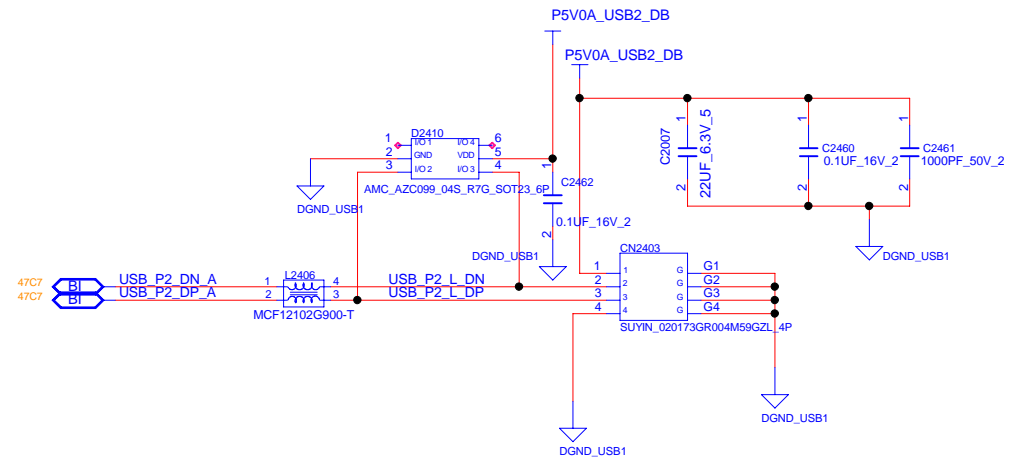
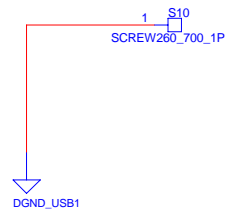
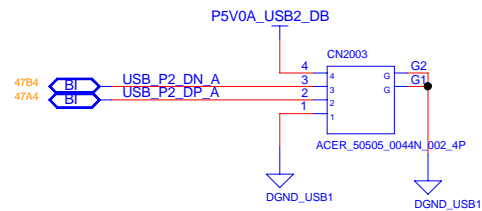
C

B

B

A

A



INVENTEC

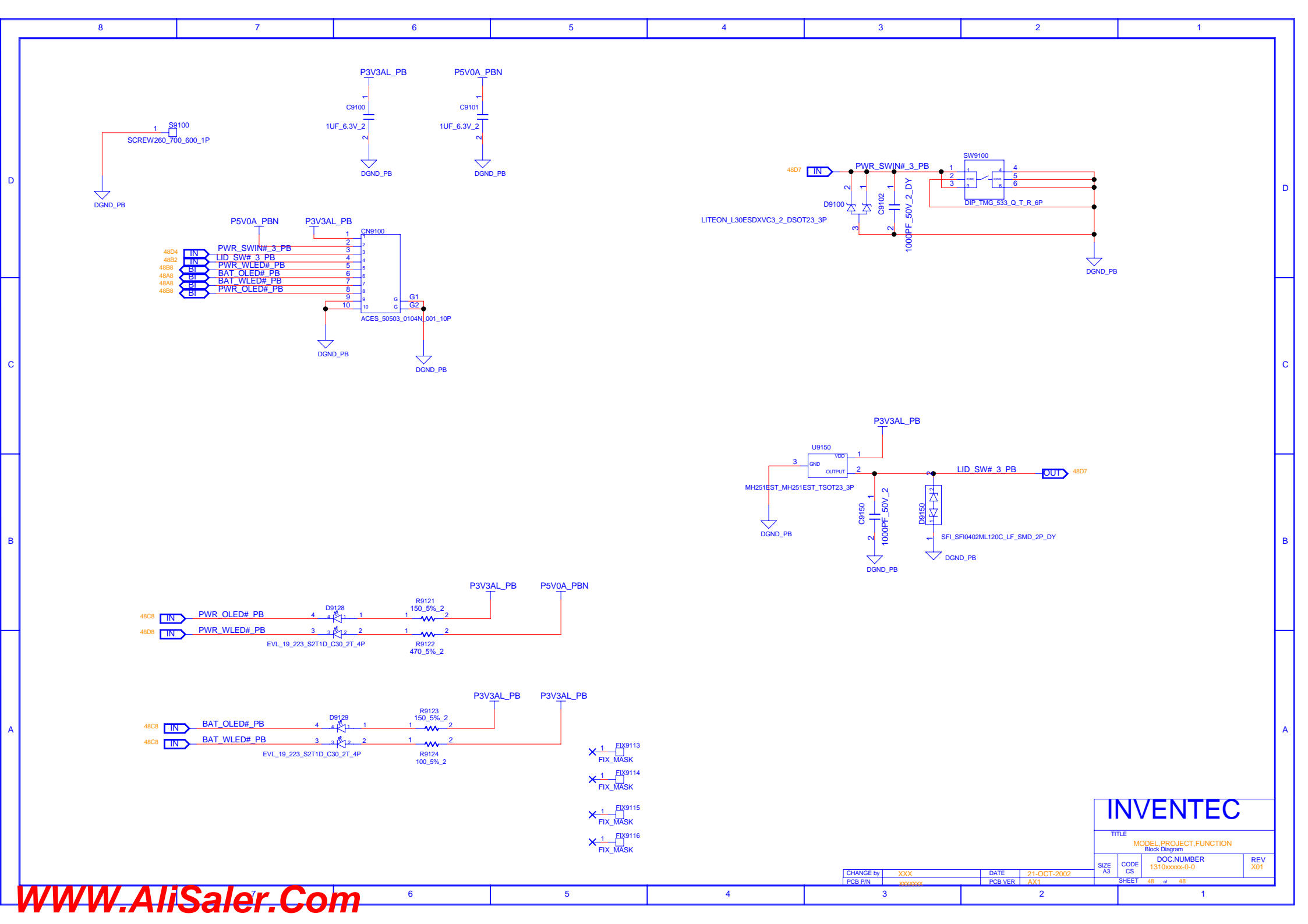
TITLE

MODEL PROJECT FUNCTION

Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET		47 of 48	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	xxxxxx	PCB VER	AX1



INVENTEC

TITLE
MODEL PROJECT FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 48 of 48			

CHANGE by PCB P/N	XXX xxxxxx	DATE PCB VER	21-OCT-2002 AX1
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